DESCRIPTION

OS100X is a highly integrated power management solution designed for wearable applications that require efficient and low quiescent current operation. OS100X contains a linear Li+ battery charge management block, two low quiescent buck regulators and 2 low quiescent low dropout linear regulators. The linear battery charger supports power path, JEITA thermal safety monitoring, step charge profiles and multiple safety timers. The buck converters in the OS1000 support DVS modes through either I2C communication or dedicated pins to switch between voltages. OS1001 buck converters do not support DVS.

OS100X contains support functions including an extremely low current off or “shelf” mode, a power button monitor with multiple functions and 4 GPIO pins which can be assigned alternate functions. OS100X also contains an 8bit ADC to allow the system to directly read the battery thermistor value and a system powering method which is used during customer system testing called Direct Mode.

OS1000 is offered in a 2.5mm x 2.0mm WLCSP Package

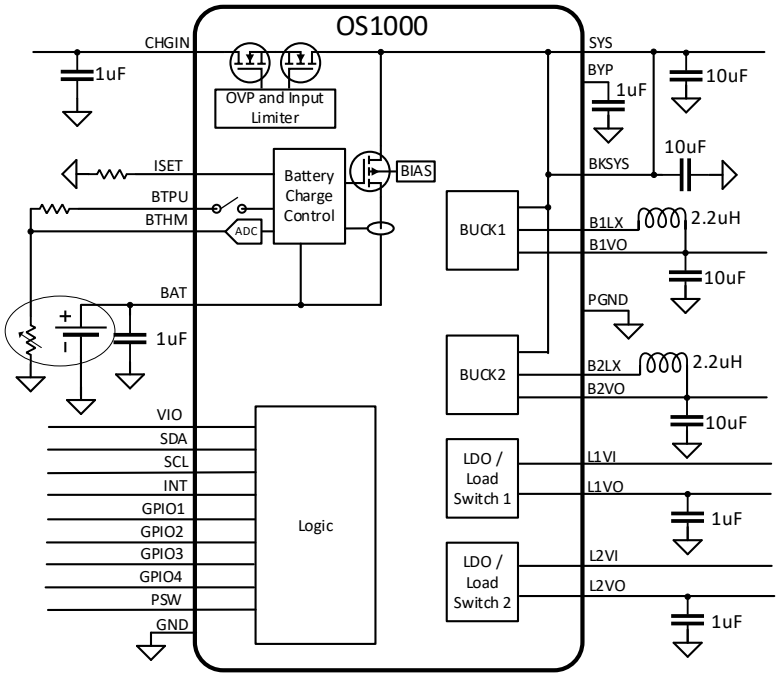
BENEFITS and FEATURES

- Li+ Battery Charge Management
  - -5.5 to +20V Input Protection
  - User configurable Step Charge
  - JEITA thermal protection
  - Pre and Fast charge safety timers
  - Power Path
- Two Low Iq Buck Converters
  - 300mA @ 0.5V to 3.0V
  - DVS capable thru I2C or GPIO (OS1000 only)
  - <500nA Iq with no load
- Two Low Iq LDO Regulators
  - Optional Load Switch mode
  - 100mA @ 0.9V to 3.3V
  - <500nA Iq with no load

APPLICATIONS

- Wearable Devices
- Medical Wearables
- TWS hearables
- IoT Devices

+



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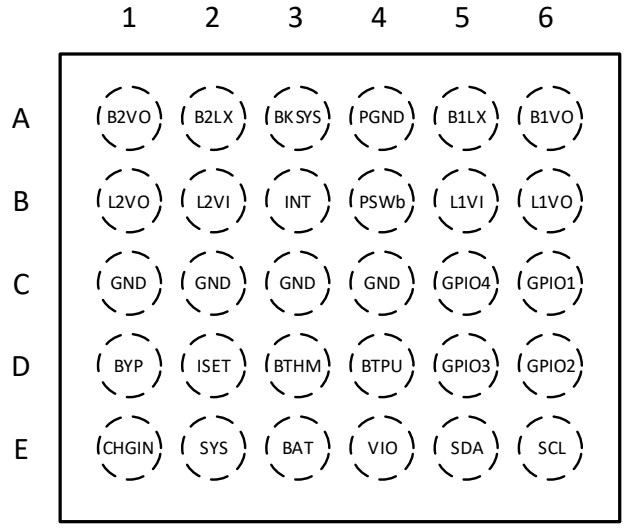
Package Drawing 30-WLCSP



2.5mm x 2.0mm 6x5 bump 0.4mm pitch. Top View

Pin List

PIN	NAME	DESCRIPTION
E1	CHGIN	Battery Charger Power Input. Bypass CHGIN with a 1uF ceramic capacitor
D4	BTPU	Li+ Thermistor bias output. Connect external Thermistor pull up resistor between BTPU and BTHM
D3	BTHM	Li+ Thermistor bias input
D2	ISET	Connect external resistor to GND to set maximum charger current.
E3	BAT	Li+ Battery Connection. Bypass BAT with a minimum 1uF ceramic capacitor
E4	VIO	Interface Power Supply Input. Bypass VIO with at least 0.1uF ceramic capacitor
E5	SDA	I2C interface data input/output. Connect SDA to VIO with a typical 10kΩ pullup resistor.
E6	SCL	I2C interface clock input. Connect SCL to VIO with a typical 10kΩ pullup resistor.
B3	INT	Interrupt open drain output. Connect INT to VIO with a typical 10KΩ pullup resistor.
C6	GPIO1	General purpose input/output. Function is defined by OTP or programmable register
D6	GPIO2	General purpose input/output. Function is defined by OTP or programmable register
D5	GPIO3	General purpose input/output. Function is defined by OTP or programmable register
C5	GPIO4	General purpose input/output. Function is defined by OTP or programmable register
B4	PSWb	Power switch input. Internal passive pull up.
E2	SYS	System load output. Bypass SYS with a minimum 10uF effective capacitance

PIN	NAME	DESCRIPTION
A3	BKSYS	Input for Buck converters. BKSYS must be externally connected to SYS. Bypass BKSYS with a minimum 10uF effective capacitance.
A5	B1LX	Buck 1 inductor drive output. Connect inductor between B1LX and B1VO with short PCB traces.
A6	B1VO	Buck 1 voltage output. Bypass B1VO with 10uF effective capacitance
A2	B2LX	Buck 2 inductor drive output. Connect inductor between B2LX and B2VO with short PCB traces.
A1	B2VO	Buck 2 voltage output. Bypass B2VO with 10uF effective capacitance
B5	L1VI	LDO 1 Voltage Input. Bypass L1VI with 1uF effective capacitance. The capacitor may be shared with the power source of L1VI if the capacitor is within 1cm of L1VI.
B6	L1VO	LDO 1 voltage output. Bypass L1VO with 1uF effective capacitance
B2	L2VI	LDO 2 Voltage Input. Bypass L2VI with 1uF effective capacitance. The capacitor may be shared with the power source of L2VI if the capacitor is within 1cm of L2VI.
B1	L2VO	LDO 2 voltage output. Bypass L2VO with 1uF effective capacitance
D1	BYP	Internal Supply. Connect 1uF effective ceramic capacitor to GND. Do not connect any external load to BYP. BYP voltage range during operation is between 3.0 and 3.6V
C1, C2, C3, C4	GND	Analog Ground. All GND and PGND pins must be connected to ground on the PCB.
A4	PGND	Power Ground. All GND and PGND pins must be connected to ground on the PCB.

Absolute Maximum Ratings

	MIN	MAX	Units
CHGIN to GND	-5.5	20	V
CHGIN to GND (30µs, ≤0.1% duty cycle)		28	V
SYS, VIO, BYP, L1VI, L2VI, INT, PSWb to GND	-0.3	6.0	V
PGND to GND	-0.3	0.3	V
ISET, BTHM, BTPU, BAT, B1LX, B1VO, B2LX, B2VO, L1VO, L2VO to GND	-0.3	V_{SYS} + 0.3	V
BKSYS	V_{SYS} -0.3	V_{SYS} + 0.3	V
SDA, SCL, GPIO1, GPIO2, GPIO3, GPIO4 to GND	-0.3	V_{VIO} + 0.3V	V
Operating Ambient Temperature	-40	85	C
Storage Temperature	-55	150	C

ESD Ratings

Pin	Conditions		Value	Units
All Pins	Human Body Model (JS-001)		±1.5	kV
	Charged Device Model (JS-002)		±500	V
CHGIN to GND	With ≥0.1uF ceramic capacitor to GND	IEC61000-4-2 Air Gap	±15	kV
		IEC61000-4-2 Contact	±8	kV

Electrical Characteristics

Global Conditions

V_{BAT}= 2.7V to 4.9V, V_{CHGIN}=0V or 4.2V to 6.5V, T_A = -40C to 85°C unless otherwise noted. Typical values are T_A = 25C, V_{BAT} = 3.6V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF}=1uF, C_{SYS_EFF} = 10uF, C_{BUCK_EFF} = 10uF, C_{LDO_EFF} = 1uF, R_{ISET}=800ohms

General

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
Shutdown Quiescent Current	I_{BATQ}	Shelf mode enabled		100		nA
		Shelf mode enabled, T_J=50C			500	
Bat Operating Current	I_{BAT}	V_{CHGIN}=0V, Buck1 and LDO1 enabled, no loads		2.5		µA
		V_{CHGIN}=0V, Buck1 and LDO1 enabled, no loads, T_J=50C			3.4	
		V_{CHGIN}=0V, Buck1 and Buck2 enabled, LDO1/2 in load switch mode		3.4		
CHGIN Current Direct Mode	I_{CHGIN_DM}	Direct Mode Enabled, V_{CHGIN} < V_{BAT}		50	70	µA
PSWb pullup	R_{PSW}			100		kΩ
PSWb Debounce time	t_{PSWbDB}	When not in Shelf Mode		1		ms

PSWb High Input Threshold	VIH_PSWb	Relative to internal supply	62.9% of VDD			V
PSWb Low Input Threshold	VIL_PSWb	Relative to internal supply			37% of VDD	V
Die Over Temperature Shutdown	T_{SD}	Temperature at which all functions are disabled except I2C interface		150		°C
Bat Startup Voltage	$V_{BATSRTUP}$	V_{CHGIN}=0V, voltage rising		2.65		V
SYS UVLO Threshold	$V_{SYSUVLO}$	SYSUVLO=00, V_{SYS} falling	2.6	2.7	2.8	V
		SYSUVLO=01, V_{SYS} falling	2.8	2.9	3.0	
		SYSUVLO=10, V_{SYS} falling	2.9	3.0	3.1	
		SYSUVLO=11, V_{SYS} falling	3.1	3.2	3.3	
Sys UVLO Hysteresis	$V_{SYSUVLOHYS}$	V_{SYS} rising		100		mV
SYS UVLO Debounce Time	$T_{SYSUVLODB}$			20		µs
Clock Period Accuracy			-5		5	%

Input Limiter and OVP

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
CHGIN vs GND Threshold	V_{CHGIN_DET}	V_{CHGIN} rising	3.8	4.0	4.2	V
CHGIN vs BAT Valid Threshold	$V_{CHGIN\_BAT\_R}$	V_{CHGIN} – V_{BAT} rising		100	150	mV
CHGIN vs BAT Invalid Threshold	$V_{CHGIN\_BAT\_F}$	V_{CHGIN} – V_{BAT} falling	0	20	40	mV
CHGIN Detect Debounce time	t_{CHGIN_DEB}			50		ms
CHGIN Overvoltage Threshold	V_{CHGIN_OV}	V_{CHGIN} rising	6.0	6.3	6.6	V
CHGIN Overvoltage Hysteresis	$V_{CHGIN\_OV\_HYST}$	V_{CHGIN} falling		200		mV
CHGIN bleeder resistance to GND	R_{CHGIN}			20		kΩ
CHGIN Current Limit	I_{CHGIN_LIM}	CHGInLim = 0	410	450	490	mA
		CHGInLim = 1	900	1000	1100	
SYS Voltage Min Limit	$V_{SYSMINLIM}$		3.7	3.8	3.9	V
SYS Regulation Voltage Max	$V_{SYSREGMAX}$			V_{BAT} + 0.25		V
SYS Protection Voltage Limit	$V_{SYSMAXPROT}$			4.9	5.0	V
CHGIN to SYS resistance	$R_{CHGINSYS}$	V_{CHGIN}=4.5V		0.2	0.3	Ω
CHGIN Soft Start	$t_{CHGINSS}$			1		ms
CHGIN Thermal Shutdown Temp	$T_{CHGINSD}$	Temperature where CHGIN current turned off, Temp rising		140		°C

CHGIN Thermal Shutdown Temp Hysteresis	$T_{CHGINSD\_HYS}$			30		°C

Charger

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
BAT to SYS On Resistance	R_{BATSYS}	V_{BAT}=4.2V		45	65	mΩ
BAT to SYS Current Limit	I_{SYSLIM}	V_{BAT}=4.2V, SYS overcurrent protection. OS100X enters shelf mode after shutdown.	1.5	3		A
Charger Pause Temperature	T_{CHGPS}	CHGTempPs =00, T_{CHGPS} rising		60		°C
		CHGTempPs =01, T_{CHGPS} rising		80		
		CHGTempPs =10, T_{CHGPS} rising		100		
		CHGTempPs =11, T_{CHGPS} rising		130		
Charger Pause Temp Hysteresis	T_{CHGPS_HYS}			20		°C
Charger Reduction Temperature	T_{CHGRED}	T_{CHGRED} rising		T_{CHGPS} - 10		°C
Charger Reduction Temp Hysteresis	T_{CHGRED_HYS}			5		°C
BAT to SYS Path On	$V_{B\text{-}S\_ON}$	V_{SYS} falling below V_{BAT}	0	12.5	25	mV
BAT to SYS Path Off	$V_{B\text{-}S\_OFF}$	V_{SYS} rising above V_{BAT}			0	mV
Charger Soft Start				1		ms
Pre-Charge Current	I_{PRECHG}	ICHGPre=00, (% of I_{FSTCHG})	2.5	3.12	3.75	%
		ICHGPre=01, (% of I_{FSTCHG})	5.62	6.25	6.88	
		ICHGPre=10, (% of I_{FSTCHG})	12	12.5	13	
		ICHGPre=11, (% of I_{FSTCHG})	24.5	25	25.5	
Pre-Charge Threshold	V_{CHGPRE}	VCHGPre=00, V_{CHGPRE} rising	2.08	2.1	2.12	V
		VCHGPre=01, V_{CHGPRE} rising	2.38	2.4	2.42	
		VCHGPre=10, V_{CHGPRE} rising	2.67	2.7	2.73	
		VCHGPre=11, V_{CHGPRE} rising	2.97	3.0	3.03	
Pre-Charge Voltage Hysteresis	$V_{CHGPREHYST}$			100		mV
Step Fast Charge Current Reduction	$I_{CHGFSTRD}$	StpChgI=000 (% of I_{CHGFST})	49.5	50	50.5	%
		StpChgI=001 (% of I_{CHGFST})	59.5	60	60.5	
		StpChgI=010 (% of I_{CHGFST})	69.5	70	70.5	
		StpChgI=011 (% of I_{CHGFST})	79.5	80	80.5	
		StpChgI=100 (% of I_{CHGFST})	84.5	85	85.5	
		StpChgI=101 (% of I_{CHGFST})	89.5	90	90.5	
		StpChgI=110 (% of I_{CHGFST})	94.5	95	95.5	
		StpChgI=111 (% of I_{CHGFST})		100		
ISET Current Coefficient	K_{ISET}	Charge Current=K / R_{ISET} R_{ISET} ≤ 2400Ω, StpChgI=111, FCHGRd=00	228	240	252	AΩ
		Charge Current=K / R_{ISET} R_{ISET} > 2400Ω	222	240	258	

		StpChgI=111, FCHGRd=00					
Fast Charge Current Range	I_{CHGFST}			5		500	mA
ISET Scaling Factor		FCHGRd=01			50		%
		FCHGRd=10			25		
		FCHGRd=11			12.5		
Battery Regulation Voltage	V_{BATREG}	Set in 4.6875mV increments		3.6		4.65	V
Bat Reg Voltage Accuracy		T_A=25C		-0.3		0.3	%
		25C<T_A<85C		0.6		0.6	
Battery Recharge Start Threshold	$V_{BATTRSRT}$			148.5	150	151.5	mV
Charge Done Threshold	$I_{CHGDONE}$	ChgDone=00 (% of I_{CHGFST}),	I_{CHGFST}= 50-450mA	1.5	2.5	3.5	%
		ChgDone=01 (% of I_{CHGFST})	I_{CHGFST}= 5-450mA	4	5	6	
		ChgDone=10 (% of I_{CHGFST})		8.5	10	11.5	
		ChgDone=11 (% of I_{CHGFST})		18	20	22	
Prequalification TImer	$t_{PREQUAL}$	PreQualTmr=00			30		min
		PreQualTmr=01			60		
		PreQualTmr=10			90		
		PreQualTmr=11			120		
Fastcharge Timer	t_{FSTCHG}	FstChgTmr=00			1.5		hour
		FstChgTmr=01			4		
		FstChgTmr=10			6.5		
		FstChgTmr=11			9		
Topoff Timer	t_{TOPOFF}	TopOffTmr = 00			0		min
		TopOffTmr = 01			10		
		TopOffTmr = 10			20		
		TopOffTmr = 11			30		
JEITA Warm/Cool Voltage	V_{JTAV}	JtaWarmV or JTACoolV = 0b01			50		mV
		JtaWarmV or JTACoolV = 0b10			150		
		JtaWarmV or JTACoolV = 0b11			250		
JEITA Threshold Accuracy		Accuracy for JEITACold, Netcool, JEITAWarm and JEITAHot			±2		%

Buck1 and Buck2

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
No load operating input current	$I_{BxVI\_NO\_LOAD}$	I_{BxVO} = 0µA, V_{BxVO} = 1.8V		600		nA
No load operating input current	$I_{BxVI\_NO\_LOAD}$	I_{BxVO} = 0µA, V_{BxVO} = 1.2V		600		nA
Shutdown Current	$I_{BxVI\_SHUTDOWN}$	V_{BxVO}=0V		50		nA

Output Voltage Accuracy	V_{OUT}	I_{BxVO} = 1mA	-2		2	%
DC Output line regulation	V_{OUT}	I_{BxVO} = 100mA, over V_{BxVI} voltage range		1		%
Soft Start	t_{SS}			1.7		ms
Turn on delay time	t_{DLYON}	GPIO control, V_{BxVO}=1.2V, Time from GPIO rising edge to 10% of V_{BxVO}		1		ms
High side switch RDS ON	R_{HIGH}			0.22		Ω
Low Side Switch RDS ON	R_{LOW}			0.18		Ω
Continuous Output Current	I_{BOUTC}				300	mA
Overload Output Current	$I_{BOUTMAX}$	Up to 10ms duration	400			mA
VOUT Discharge Resistance	R_{DIS}		50	100	150	Ω

LDO / Load Switch

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
Allowed Input Voltage	V_{LDOIN}	LDO Mode	1.71		5.5	V
		Load Switch Mode	0		5.5	
Quiescent Current	I_{LDOON}	LDO Mode, No Load		700		nA
		Load Switch Mode		600		
Quiescent Current Dropout	I_{LDOOND}	LDO Mode, V_{LxVI}=3.0V, Programmed for 3.3V		1.9	6	µA
Maximum Output Current	I_{OUTMAX}	LDO Mode	100			mA
Output Voltage Accuracy		LDO Mode, V_{OUT}=2.5V, I_{OUT}=1mA	-2		2	%
Dropout voltage	$V_{LDODROP}$	LDO Mode, V_{LxVI}=3.0V, I_{LxVO}=100mA		60	110	mV
Line Voltage Regulation error	$V_{LDOLIREG}$	LDO Mode, V_{LxVI}=3.0V to 5.5V, V_{LxVO}=2.5V		±0.2		%/V
Load Voltage Regulation error	$V_{LDOLOREG}$	LDO Mode, V_{LxVI}=3.6V, V_{LxVO}=1.8V, I_{LxVO}=100uA to 100mA		0.03		%/mA
Passive Discharge Resistance	R_{LDOOUT}			100		Ω
On Resistance	I_{LDORON}	Load Switch Mode, I_{LDOOUT}=5mA		0.3	0.75	Ω
Turn On Time	t_{LDOON}	LDO Mode, 10% to 90%, No Load, C_{LDO}=1uF		1.7	2.5	ms
		Load Switch Mode, 10% to 90%, No Load, C_{LDO}=1uF		50		µs
Short Circuit Current	I_{LDOSC}	LDO Mode	200	300	500	mA
		Load Switch Mode	150	450	500	
Output Noise	$V_{LDONOISE}$	LDO Mode, 10Hz to 100kHz, V_{LxVI}=3.6V, V_{LxVO}=1.8V		150		μV_{RMS}
Leakage IN to OUT	$I_{LDOLEAK}$	LDO disabled, V_{LxVI}=3.6V, V_{LxVO}=0V		20	360	nA
		Load Switch disabled, V_{LxVI}=1.8V, V_{LxVO}=0V		20	360	nA

I2C and GPIO Interface

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
Low Level Input Voltage	V_{IL}				0.3*VIO	V
High Level Input Voltage	V_{IH}		0.7*VIO			V
Low Level Output Voltage	V_{OL}	Sinking 5mA			0.4	V
High Level Output Voltage	V_{OH}	GPIO pins only, Sourcing 1mA	VIO-0.4			V
GPIO Pull Resistance	R_{GPIO}			150		KΩ
GPIO Debounce Time	t_{GPIO_DB}	GPIO pins in input mode		1		µs
Pulse Width of Suppressed Spikes	t_{SPIKE}	SCL and SDA only			50	Ns
Input leakage Current	I_{INLEAK}	VIO=3.0V, V_{SDA}/V_{SCL}/V_{GPIOx}=(0V or VIO)		±1		µA
I2C SCL Frequency	f_{SCL}				1000	kHz
Hold Time Repeated START	$t_{HD;STA}$	After this period, the first clock pulse is generated	0.26			µs
Min Low Clock Period	t_{SCLLOW}		0.5			µs
Min High Clock Period	$t_{SCLHIGH}$		0.26			µs
Repeated START Setup Time	$t_{SU;STA}$		0.26			µs
Data Setup Time	$t_{SU;DAT}$		50			Ns
Output Fall Time	t_{OFALL}	VIO=1.8V, 70% to 30%			120	Ns
Allowed Input Rise Time	t_{IRISE}	VIO=1.8V, 70% to 30%			120	ns
STOP Setup time	$t_{SU;STO}$		0.26			µs
Bus Free Time	t_{BUF}	Between STOP and START condition	0.5			µs
Allowed Capacitance Load	C_{Bh}	SCL/SDA only			550	pF
Data Valid Time	$t_{VD;DAT}$				0.45	µs
Data Valid Ack Time	$t_{VD;ACK}$				0.45	µs
Low Level Noise Margin	V_{nL}	For each connected device (including hysteresis)	0.1*VIO			V
High Level Hoise Margin	V_{nH}	For each connected device (including hysteresis)	0.2*VIO			V
Spike Filter	t_{SP}				50	ns

Typical Operating Characteristics

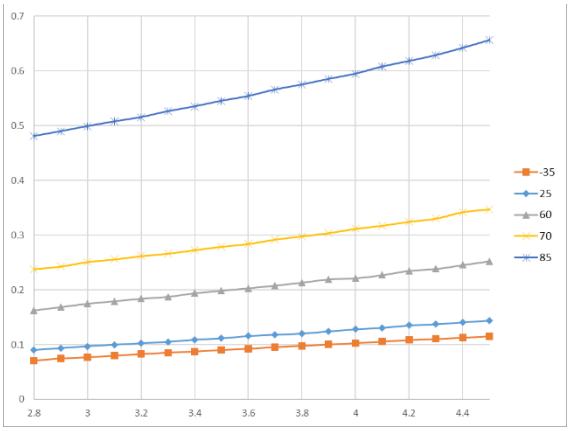


Figure 1 Shelf Mode I_{BAT} (uA) vs. V_{BAT} over Temperature

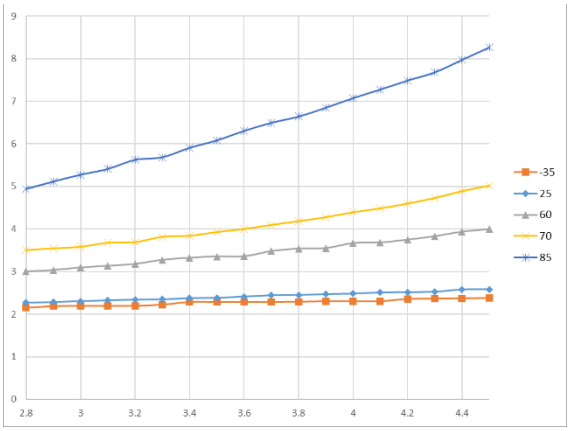


Figure 2 I_{BAT} (uA) vs V_{BAT} over Temperature with BUCK1=1.2V, BUCK2=1.8V, LDOs disabled, no Loads

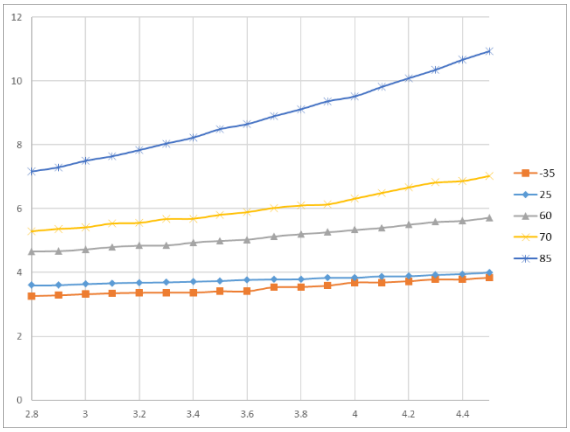


Figure 3 I_{BAT} (uA) vs V_{BAT} over Temperature with BUCK1=1.2V, BUCK2=1.8V, LDO1=LDO2=1.8V, no Loads

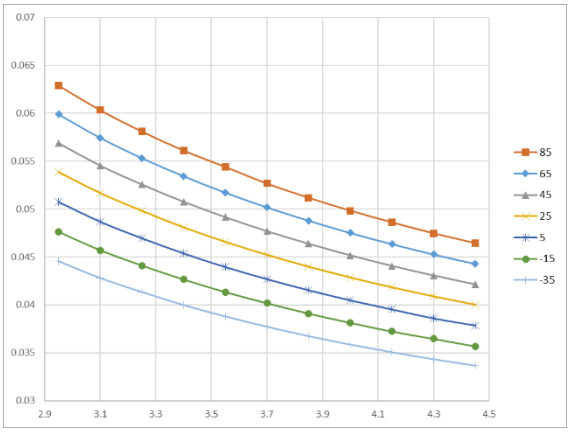


Figure 4 SYS to BAT On Resistance (ohms) vs V_{BAT} over Temperature

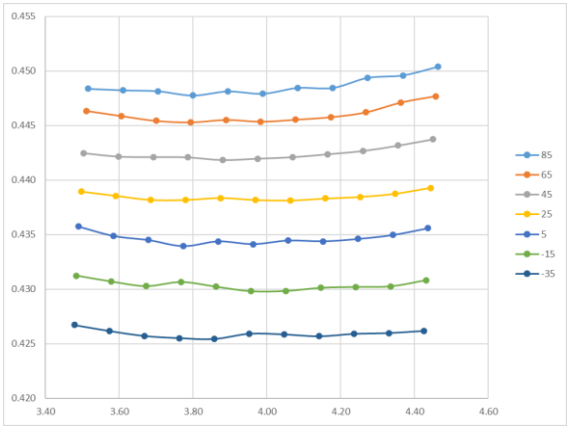


Figure 5 CHGIN Current Limit (amps) vs V_{SYS} for CHGInLim=0 over Temperature

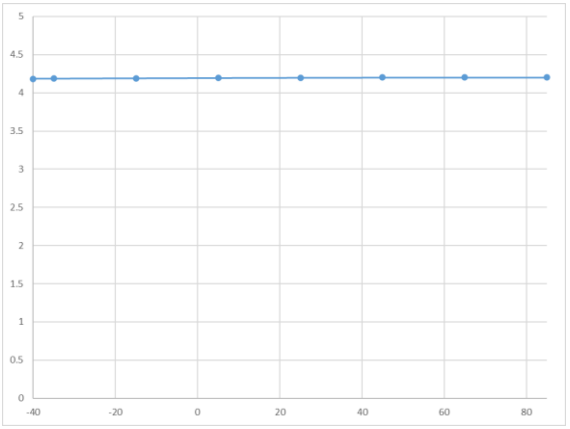


Figure 6 Battery Charger Regulation Voltage vs Temperature

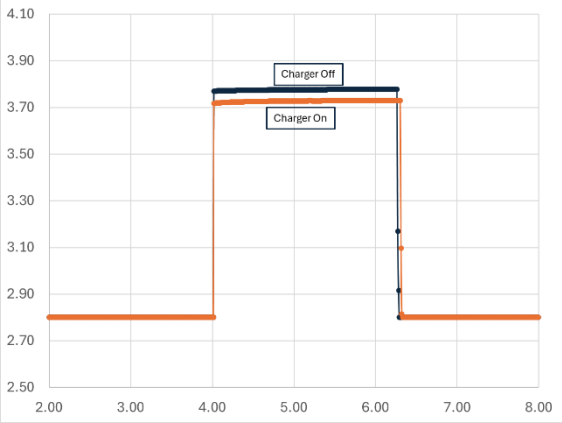


Figure 7 V_{SYS} vs V_{CHGIN}

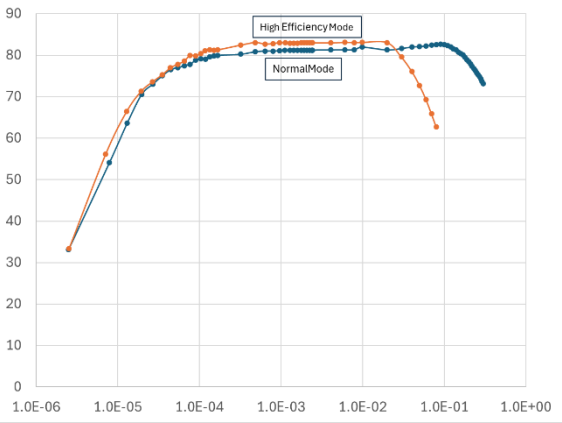


Figure 8 Buck Efficiency vs load (mA) V_{SYS}=3.0V, V_{BUCK}=0.55V

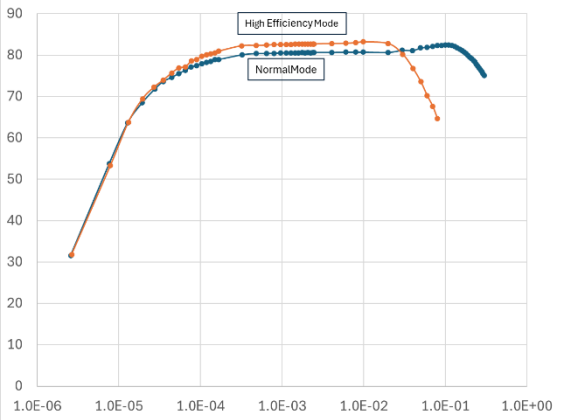


Figure 9 Buck Efficiency vs load (mA) V_{SYS}=3.6V, V_{BUCK}=0.55V

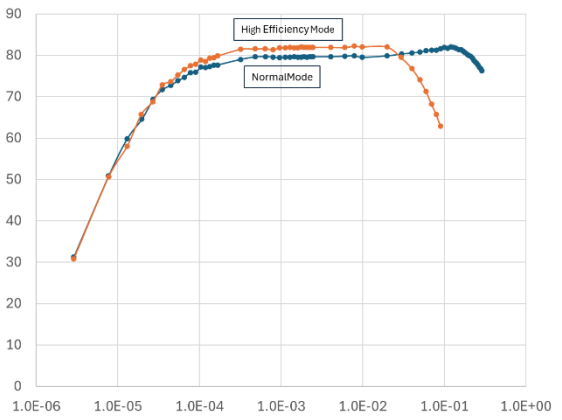


Figure 10 Buck Efficiency vs load (mA) V_{SYS}=4.2V, V_{BUCK}=0.55V

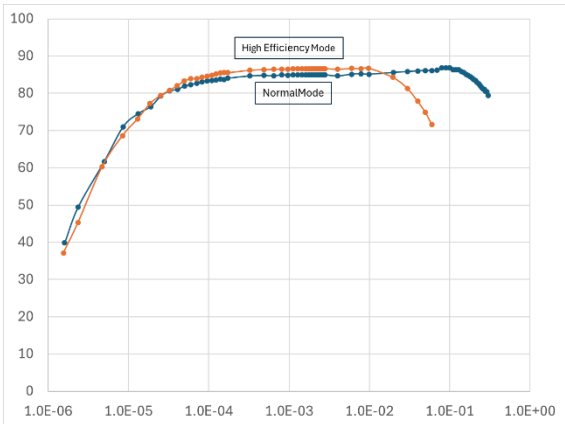


Figure 11 Buck Efficiency vs load (mA) V_{SYS}=3.0V, V_{BUCK}=0.9V

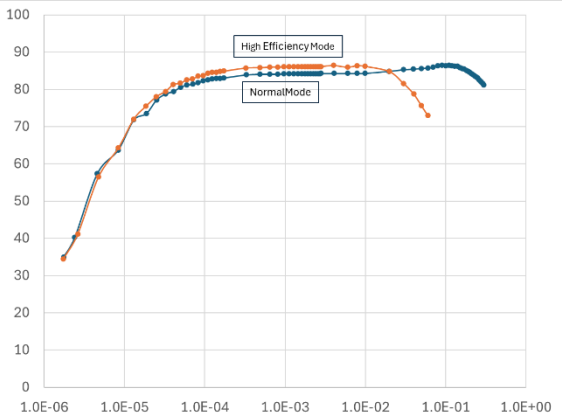


Figure 12 Buck Efficiency vs load (mA) V_{SYS}=3.6V, V_{BUCK}=0.9V

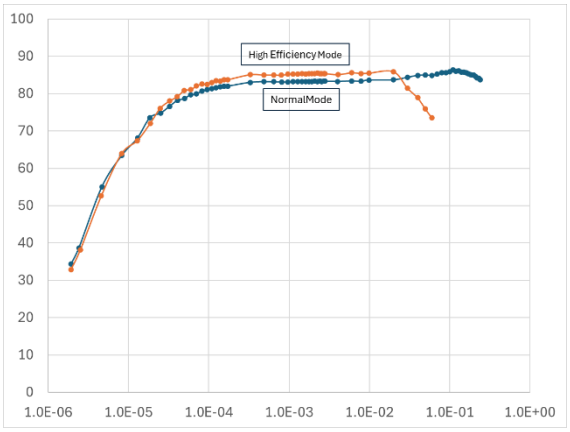


Figure 13 Buck Efficiency vs load (mA) V_{SYS}=4.2V, V_{BUCK}=0.9V

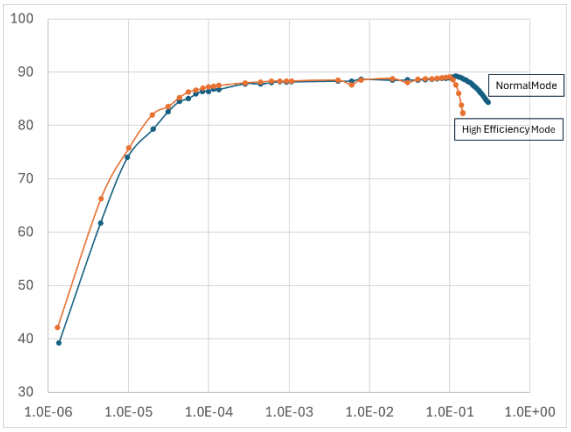


Figure 14 Buck Efficiency vs load (mA) V_{SYS}=3.0V, V_{BUCK}=1.2V

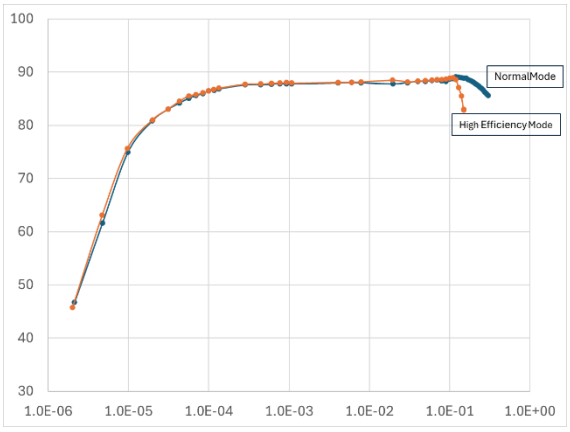


Figure 15 Buck Efficiency vs load (mA) V_{SYS}=3.6V, V_{BUCK}=1.2V

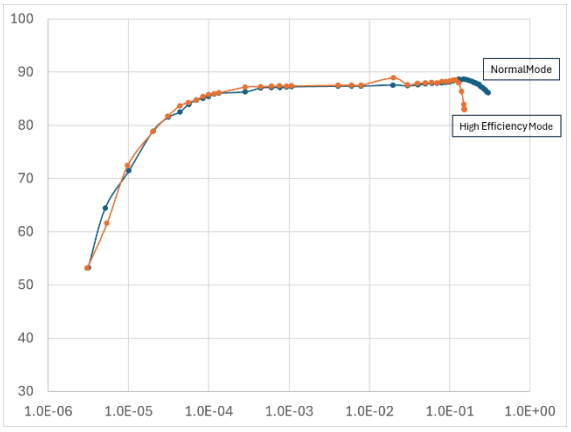


Figure 16 Buck Efficiency vs load (mA) V_{SYS}=4.2V, V_{BUCK}=1.2V

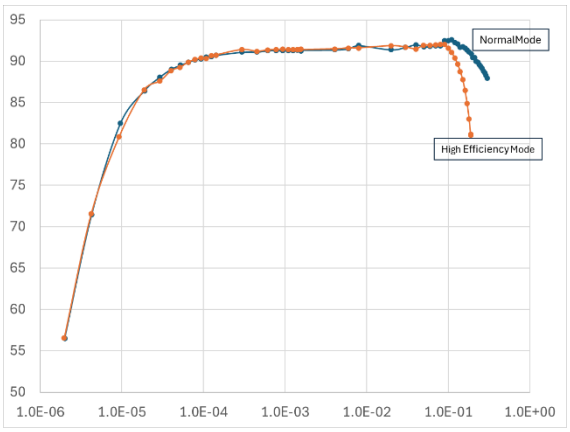


Figure 17 Buck Efficiency vs load (mA) V_{SYS}=3.0V, V_{BUCK}=1.8V

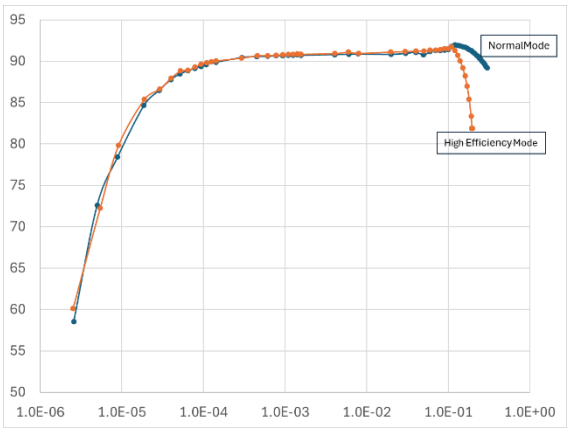


Figure 18 Buck Efficiency vs load (mA) V_{SYS}=3.6V, V_{BUCK}=1.8V

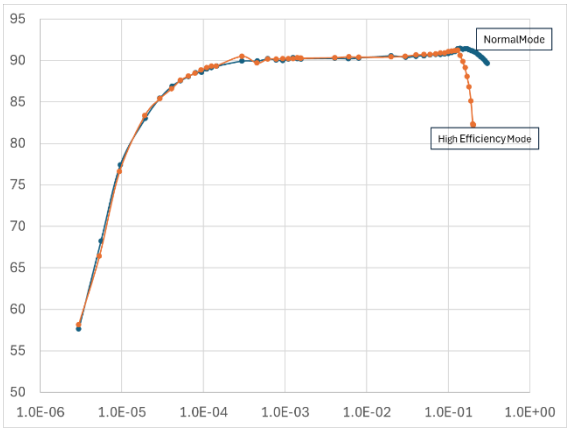


Figure 19 Buck Efficiency vs load (mA) V_{SYS}=4.2V, V_{BUCK}=1.8V

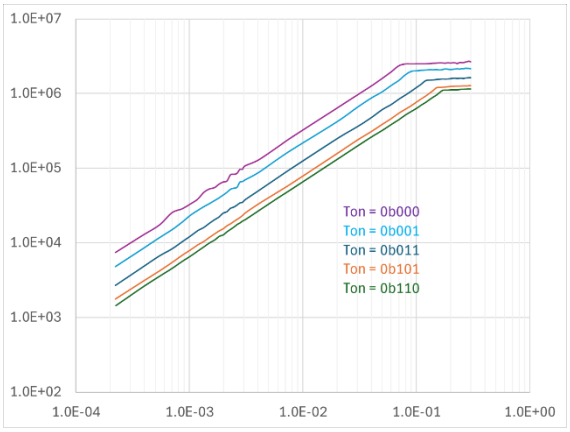


Figure 20 Buck Switching Frequency (Hz) vs Load (A)

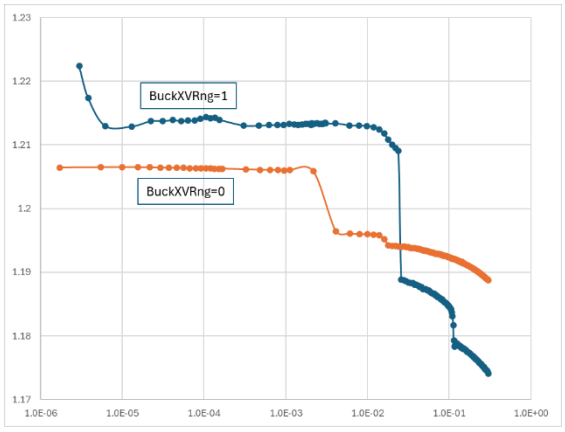


Figure 21 Buck Load Regulation V_{BUCK} =1.2V vs I_{LOAD} (A)

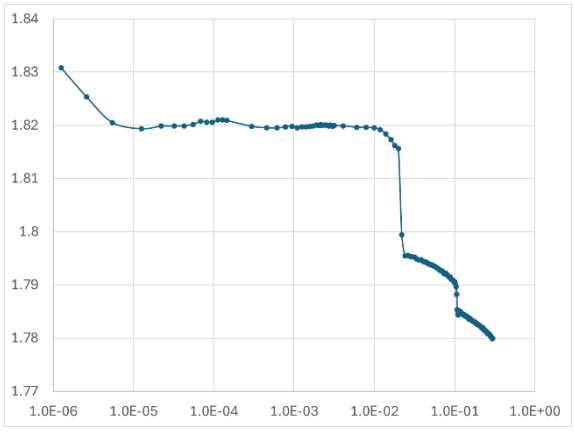


Figure 22 Buck Load Regulation VBUCK =1.8V vs ILOAD (A)

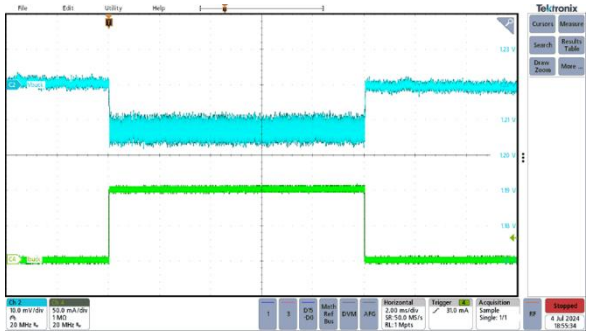


Figure 23 Buck Load Transient I_{LOAD}=0mA to 100mA, with V_{SYS}=3.6V, Ton=0b011, V_{BUCK}=1.2V

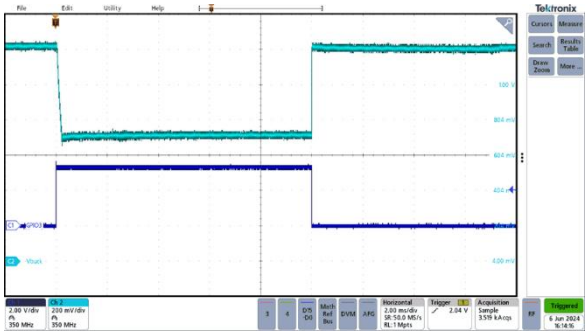


Figure 24 Buck DVS Transition by GPIO 1.2V to 0.7V to 1.2V with V_{SYS}=3.6V, Ton=0b011, no load (OS1000)

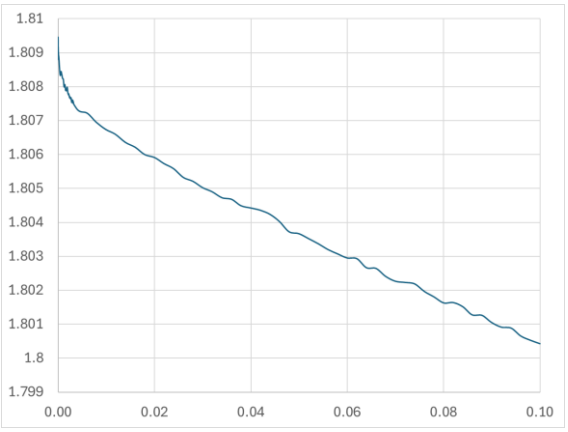


Figure 25 LDO Load Regulation vs Load (mA), V_{LDO}=1.8V, V_{SYS}=3.6V

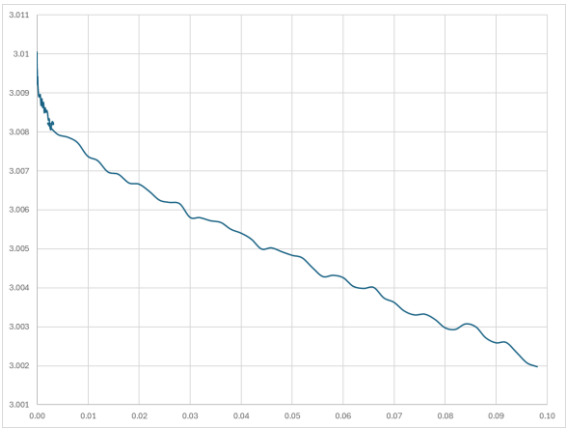


Figure 26 LDO Load Regulation vs Load (mA), VLDO=3.0V, VSYS=3.6V

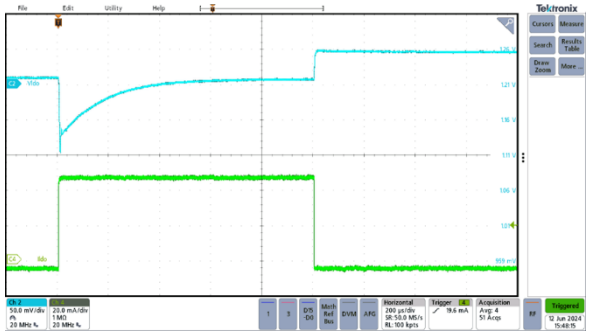


Figure 27 LDO Load Transient I_{LOAD}=0mA to 50mA, with V_{SYS}=3.6V, V_{LDO}=1.2V

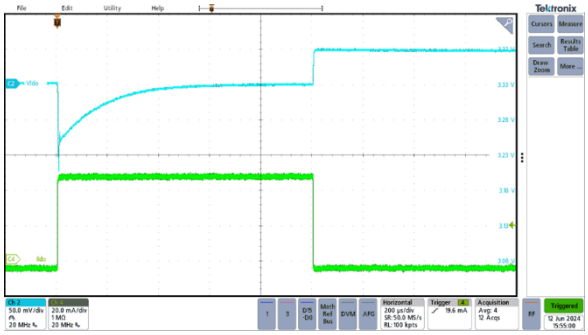


Figure 28 LDO Load Transient ILOAD=0mA to 50mA, with VSYS=3.6V, VLDO=3.0V

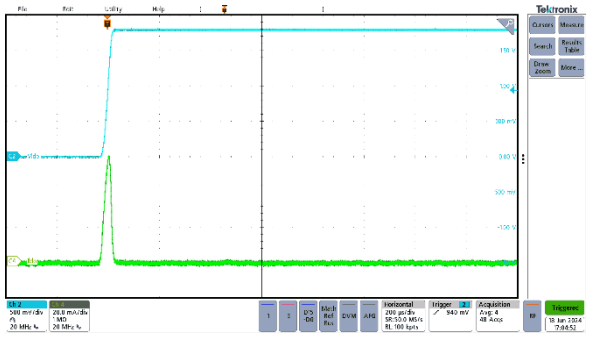
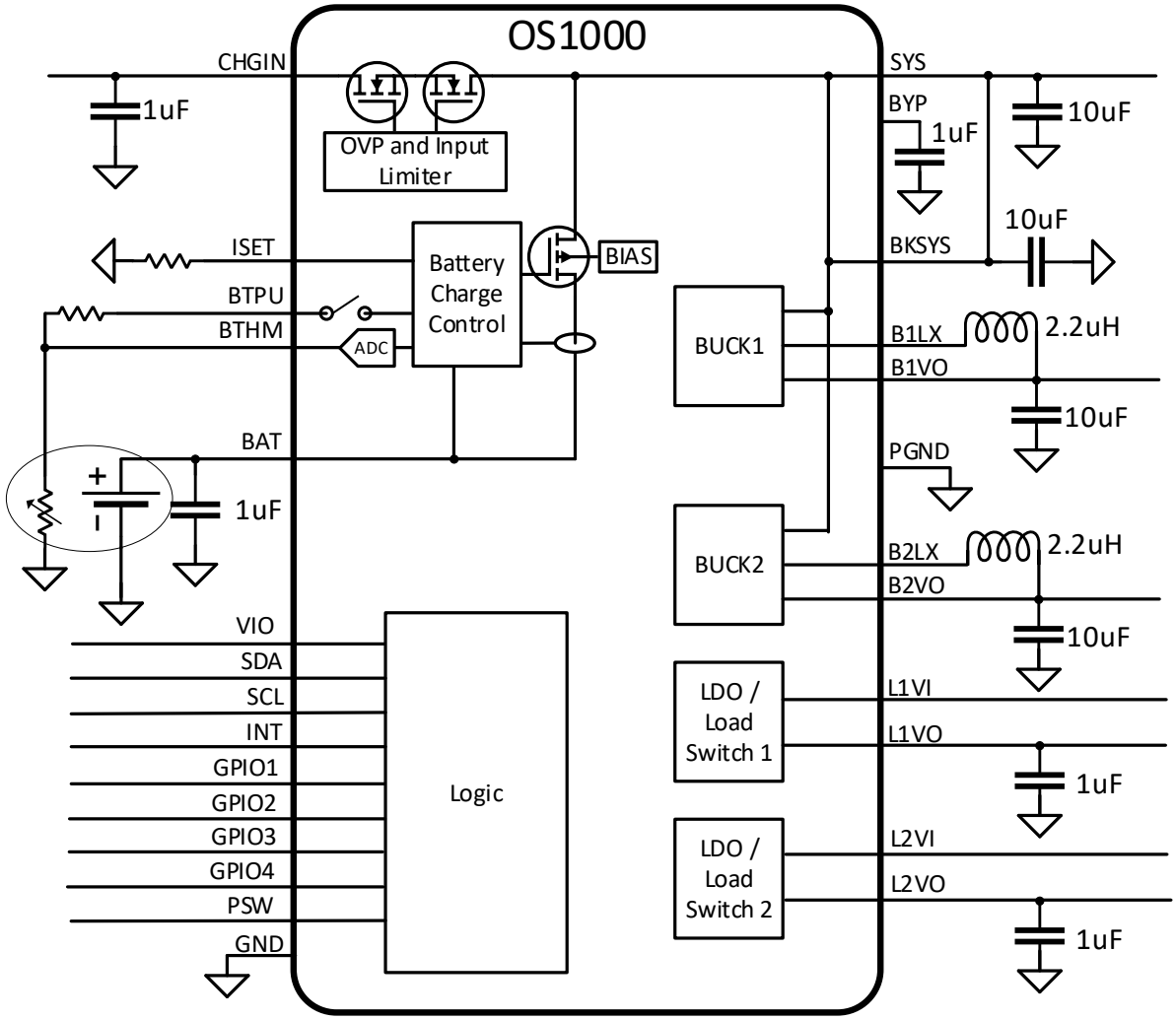


Figure 29 Load Switch Inrush Current. V_{LDO}=1.8V, C_{LDO}=4.7uF

Functional Block Diagram



Detailed Description

Startup and reset behavior

OS100X is a simple power management device which is designed to power low power draw devices (e.g. wearables, medical devices, smart rings etc.) from a Li+ battery. These devices may need to remain in an ultra-low operating current state for a long time post assembly but before a customer purchases the device and begins using it. OS100X supports this operation state with Shelf Mode.

Shelf Mode

In shelf mode, OS100X is in its lowest operating current state. OS100x is woke by attaching a power source to CHGIN or pulling PSWb low for a time greater than the wakeup time ($t_{PSWbWkTm}$) and releasing the PSWb button (PSWB pulled high) in less than the PSWb long press reset time ($t_{PSWbRsTm}$) while $V_{BAT}>V_{BATUVLO}$. When OS100X is in shelf mode, SYS is pulled to GND with a 100 ohm resistor.

Figure 30 Exit Shelf Mode due to PSWb

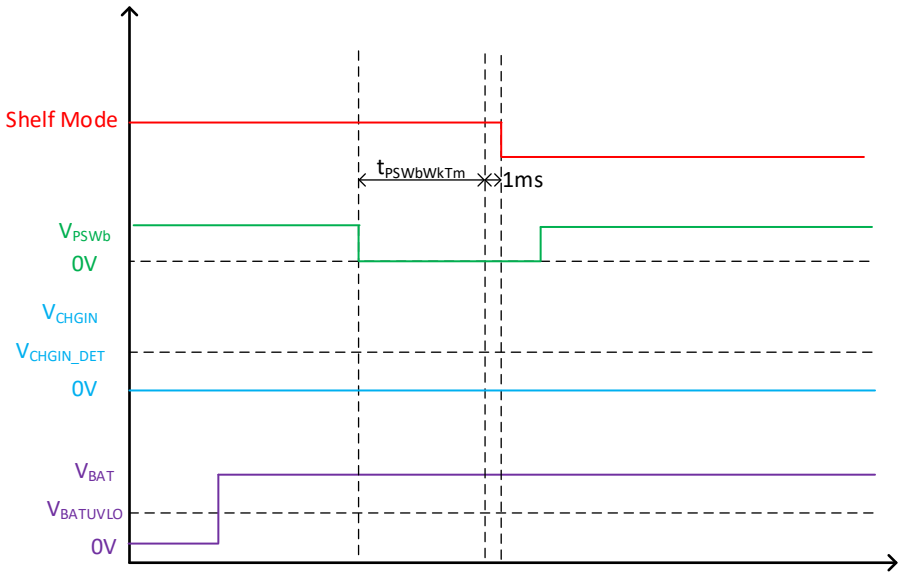
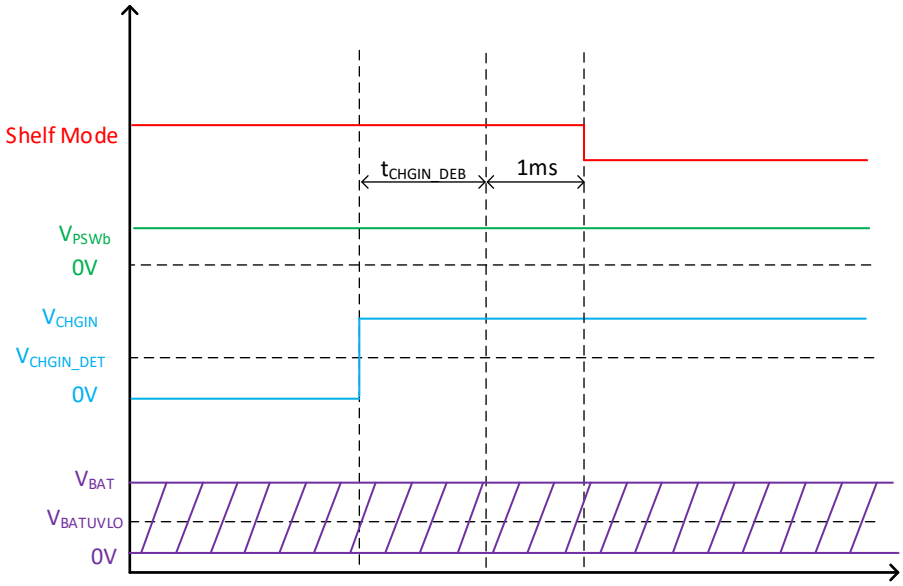


Figure 31 Exit Shelf Mode due to CHGIN attach

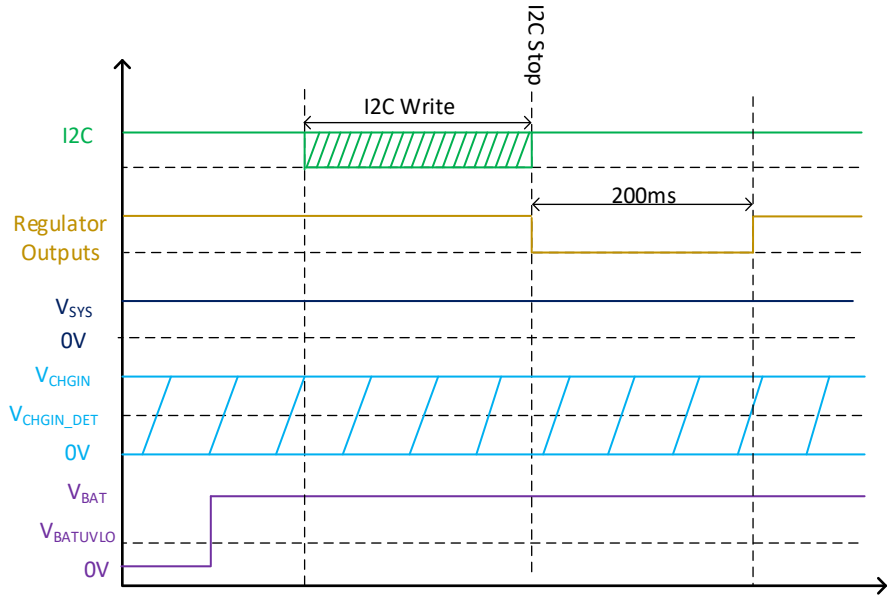


Reset

I2C Reset bit

OS100X may be reset to default operation by setting the Reset bit to 1. OS100X will reset all registers to defaults after waiting 1ms, shut off all regulators for 200ms and restart the startup sequence which will return all voltage regulators to their initial default operation state (off or on) and voltage. See Figure 32 for additional details.

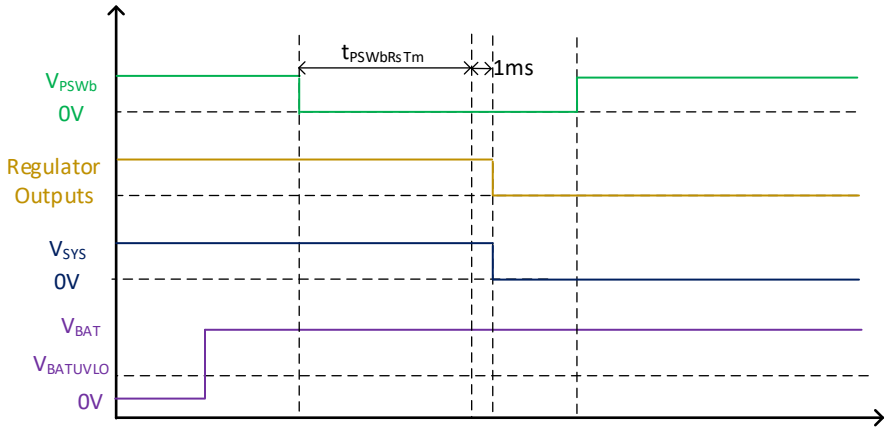
Figure 32 Reset due to I2C register write



PSWb Long Press Reset

OS100X may be used to recover from a system lockup or other error by pulling PSWb low for a time greater than $t_{PSWbRsTm}$ (up to 12s). OS100X will turn off all regulators and turn off SYS (which is discharged through 100ohm resistor) and enter shelf mode. OS100X will restart after either PSWb is pulled low for a time greater than $t_{PSWbWkTm}$ (up to 2000ms) and then released or CHGIN is attached and is valid. See Figure 33 for additional details.

Figure 33 OS100X Reset by PSWb long press



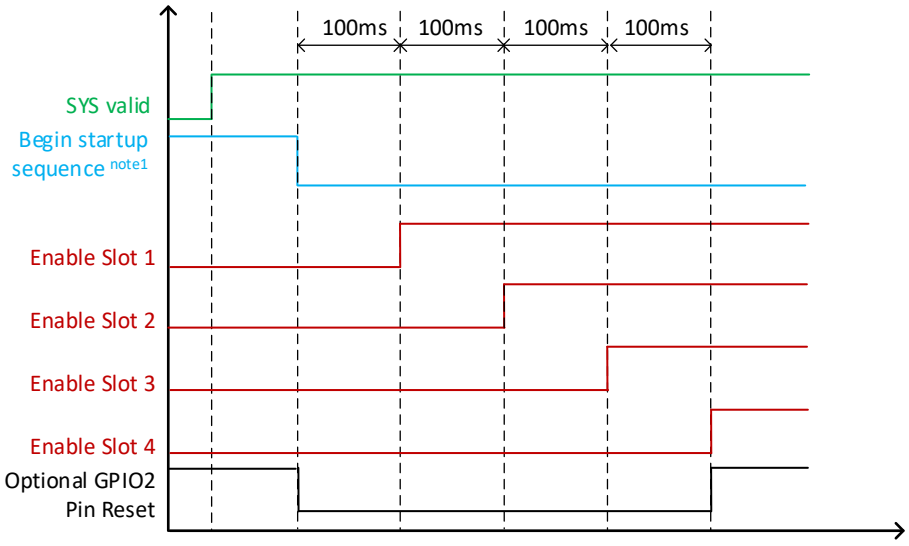
PSWb Mirror to GPIO1

GPIO1 may be configured to mirror the voltage state on PSWb with an open drain output (Pull Up voltage must be ≤ VIO). When OS100X is in normal operation mode (not Shelf Mode), PSWb is debounced with a 1ms timer.

Startup Regulator Sequencing

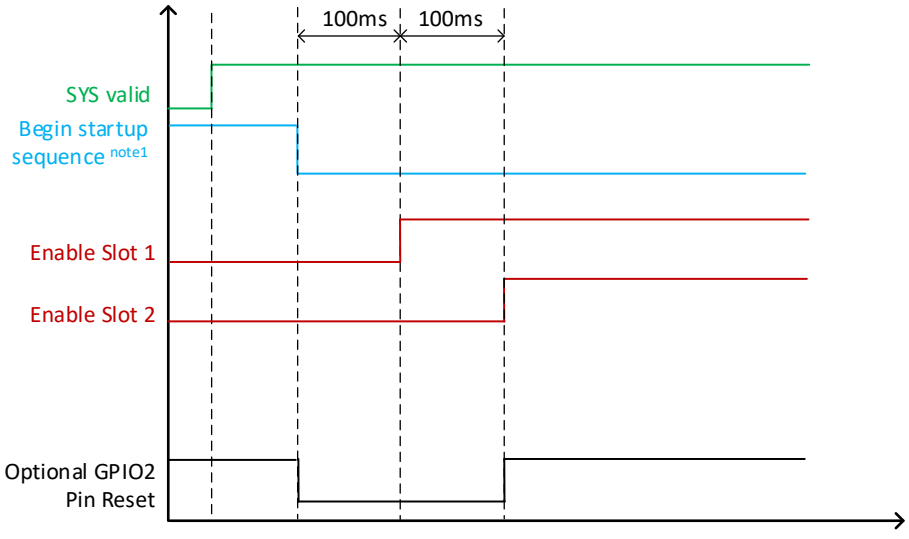
OS100X may be configured to sequence the startup of regulators in one of 4 possible time slots with one additional “dummy” slot. These time slots start after SYS becomes valid and the startup sequence is initiated by either shelf mode exit (CHGIN attach or PSWb pull down) or an OS100X reset request (PSWb long pulldown or I2C register write). The total time for startup depends on the number of slots enabled. It is also valid to program dummy slots to enable longer time between regulators.

Figure 34 Startup Sequence with 4 slots enabled



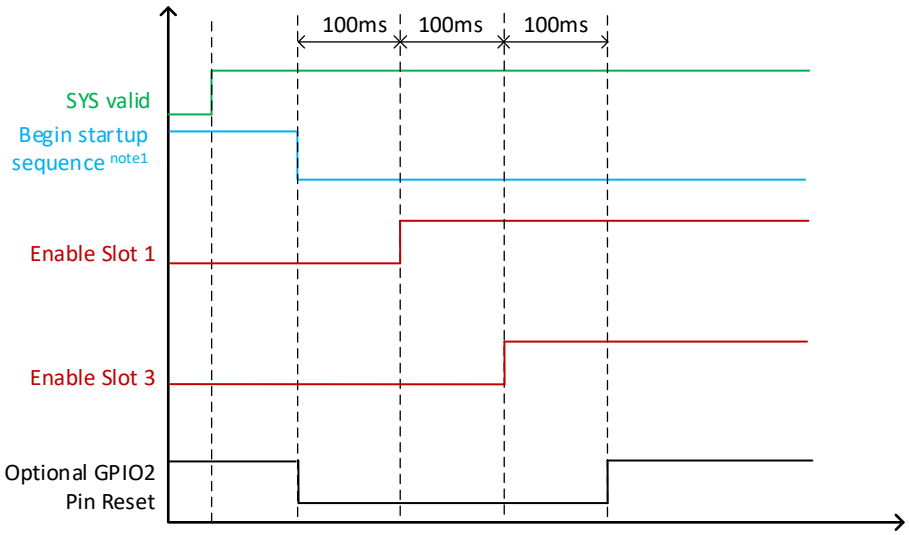
note1: Startup sequence begins after Shelf mode exit or PMIC01 reset request.

Figure 35 Startup Sequence with 2 slots enabled



note1: Startup sequence begins after Shelf mode exit or PMIC01 reset request.

Figure 36 Startup Sequence with 2 slots enabled and one dummy slot

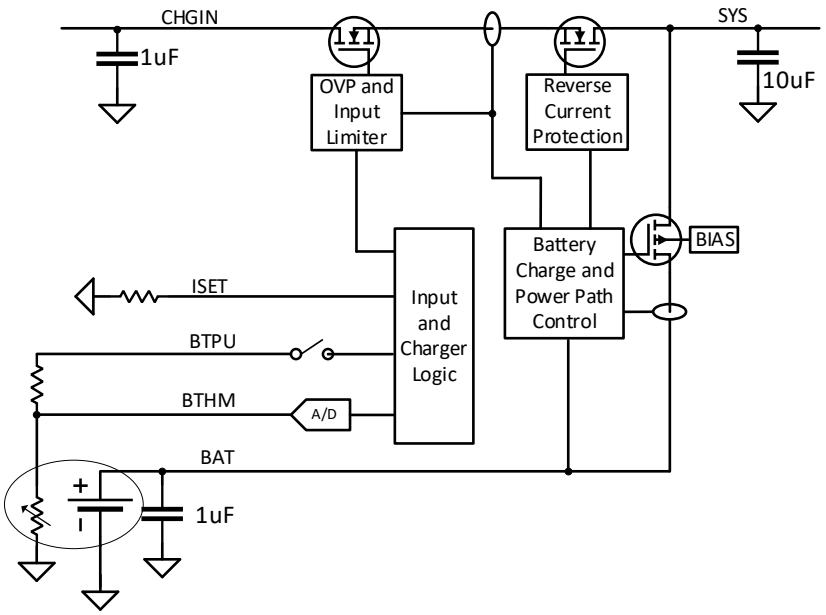


note1: Startup sequence begins after Shelf mode exit or PMIC01 reset request.

Li+ Battery Charger

OS100X contains a highly featured Li+ linear battery charger which supports overvoltage input protection, JEITA thermal management, automatic power path selection, step charging and many safety features.

Figure 37 Charger Detail



OVP and Input Limiter

OS100X takes power from external sources connected to CHGIN. CHGIN is an external pin on most end devices which must be protected against damaging events. CHGIN is protected against ESD by the addition of an external 1uF ceramic capacitor. This capacitor absorbs the ESD energy and limits the voltage surges to protect CHGIN. CHGIN also has a 20 kΩ bleed resistance to GND to remove excess charge from the input capacitor and guarantee a disconnected CHGIN is always pulled to GND. CHGIN is normally powered from a 5V source, but it is protected against dc overvoltage conditions up to 20V and reverse connected voltages down to -5.5V. If a voltage is attached that is greater than V_{CHGIN_OV}, CHGIN is disconnected from SYS and an interrupt is flagged. CHGIN continues to be monitored and if it drops below V_{CHGIN_OV} then CHGIN returns to normal operation. If CHGIN is connected to a voltage that is not valid or left unconnected, CHGIN is disconnected so no reverse current flows out of CHGIN and no voltage is present on CHGIN.

Table 1 CHGIN Valid

CHGIN State	Condition to enter, Voltage rising	Condition to exit, Voltage falling
Overvoltage	$V_{CHGIN} > V_{CHGIN\_OV}$	$V_{CHGIN} < V_{CHGIN\_OV} - V_{CHGIN\_OV\_HYST}$
Normal	$V_{CHGIN} > V_{CHGIN\_DET}$ and $V_{CHGIN} - V_{BAT} > V_{CHGIN\_BAT\_R}$	$V_{CHGIN} < V_{SYSUVLO}$ or $V_{CHGIN} - V_{BAT} < V_{CHGIN\_BAT\_F}$
Not Valid	Any other voltage or unconnected	

In normal operation, the input limiter provides a regulated current to SYS defined by CHGInLim register. The current slowly ramped (time $t_{CHGINSS}$ typical 10ms) to eliminate inrush issues charging SYS capacitance. During normal operation, if the die temperature increases to $T_{CHGINSD}$, the Input Limiter is disabled, and an interrupt is flagged. To the system and the battery charger, this event will be same as if voltage was removed from CHGIN (charger is turned off and SYS is powered from BAT).

Battery Charger

Power Path and SYS Load Switch

With CHGIN not valid, BAT is connected to SYS by a 50mΩ typical switch. When CHGIN is valid and provides sufficient current to power the load and charge the battery, this load switch is opened. If at any time the load on SYS exceeds the CHGIN current limit, the BAT to SYS load switch will be closed to supplement the CHGIN current to prevent SYS from dropping below BAT voltage. OS100X also features a power path current distribution block which seamlessly divides the current available from CHGIN to power the SYS load and to charge the battery. The load on SYS has the highest priority and the battery charge current will be reduced to maintain the SYS voltage above V_{BAT}.

SYS Voltage Regulation

OS100X utilizes a linear battery charger circuit which dissipates power defined by $P=(V_{CHGIN}-V_{BAT})/I_{CHG}$ when there is no other load on SYS. Adding loads on SYS puts additional power dissipation in the CHGIN Limiter. OS100X balances the power dissipation between the Limiter and the Charger by regulating V_{SYS} to be 3.8V until $V_{SYS}-V_{BAT}=250mV$ after which V_{SYS} is regulated to be 250mV above V_{BAT}.

VSYS voltage with no battery present depends on if the battery was not present at CHGIN attach or was removed after CHGIN attach.

- With no battery present at CHGIN attach, VSYS is regulated to 3.8V typical until a battery is attached after which it operates as described above.
- If the battery is removed after CHGIN is attached and the battery charger is enabled, V_{SYS} will rise to the protection voltage (4.9V) until either CHGIN is removed or the battery is re-attached.

Fast Charge Current Setting

The Fast charge current for OS100X is set by a resistor connected to ISET pin. The max fast charge current is set by the $I_{FCHG}=(K_{ISET}/R_{ISET})$ * FCHGRd (FCHGRd can be set through I2C to 100%, 50%, 25% or 12.5%). The actual charge current depends on the operating state of the charger and all current levels and Charge Done threshold are defined as a percentage of I_{FCHG}. If FCHGRd is set to a value other than 100%, the Charge Done threshold is also reduced by the same amount which may cause charging to not report complete and force the charge timer to expire.

Thermal Limiting

During charging if the die temperature reaches T_{CHGRD}, the charger current reduces by 50% and t_{FSTCHG} timer is doubled in an attempt to maintain the die temperature below the charger pause temperature T_{CHGPS} which pauses charging and the safety timers.

JEITA Battery Safety

OS100X includes a JEITA compliant temperature monitoring system. BTPU pin provides switched power to an external resistor divider which uses the battery pack thermistor as the lower resistor in the divider. The midpoint of the divider is connected to pin BTHM which monitors the voltage across the pack

thermistor. BTPU is switched on only when the charger is active to save power consumption. The JEITA block monitors for 5 temperature zones: cold, cool, room, warm and hot. Normal charger operation is enabled when the monitor reads room. In cold and hot, charging is disabled. In cool and warm, the charger may be programmed to reduce max current and/or max voltage as required by the battery manufacturer. The JEITA thresholds are adjustable (initial values stored in OTP and register adjustable) in 0.39% increments (8bits) from 0% to 100% of V_{BTPU}. See Figure 40 Li+ Charger State Diagram for details.

Step Charging

Lithium-ion batteries suffer capacity degradation over their lifetimes. One of the primary causes of degradation over the lifetime of a battery is due to an effect called lithium plating, which describes the formation of metallic lithium on the anode of the battery. Lithium plating has many causes, but one of the most common is when the battery is charged at high rates relative to the capacity of the battery when the battery is at a high state of charge (SOC). To combat this OS100X supports step charging which allows the max current in CC mode to be reduced as the battery approaches the CV voltage to avoid lithium plating and prolong the lifetime of the battery. Step charging is optional and may be disabled by setting StepChgIRd=0b111 (100% current) and StepChgThs=VBatReg.

Open Battery or Open Pack Protector Recovery

At initial power up, the battery voltage is checked with a small load to verify whether the pack is present or the pack protector is open. If V_{BAT}>1.2V, normal charging is started. If V_{BAT}<1.2V, then a test loop is run where the battery is charged with $I_{PREQUAL}$ for 1s and then the battery is loaded for 50ms and checked if V_{BAT}>1.2V. If V_{BAT}>1.2V then normal charging is started. If not, the loop is repeated until the $t_{PREQUAL}$ timer elapsed. If BAT remains open, then charging is disabled and the charger state machine enters the Timer Fault state.

Battery Removal Detection

The battery is detected as removed if the thermistor is removed from the BTHM pin. The removal is detected by BTHM pulled to greater than 95% of the voltage on BTPU which is higher than any normal operating condition of a thermistor. The status of the battery present threshold is indicated in Status2 register bit BatPrstSt. If there is no battery detected (voltage on BTHM greater than 95% of V_{BTPU}), the charger state machine is disabled until the thermistor is detected. Then the charger state machine restarts from state Charger Off (CHGStatus=0b00000).

ISET Resistor Fault Detection

If ISET is open or shorted to GND, the charger will not operate correctly and could damage the battery. OS100X detects this condition and forces the charger to turn off but all other functions continue to operate. OS100X will flag the error as code 0x01110 in the ChgSt register.

Figure 38 Charger Voltage and Current Profile

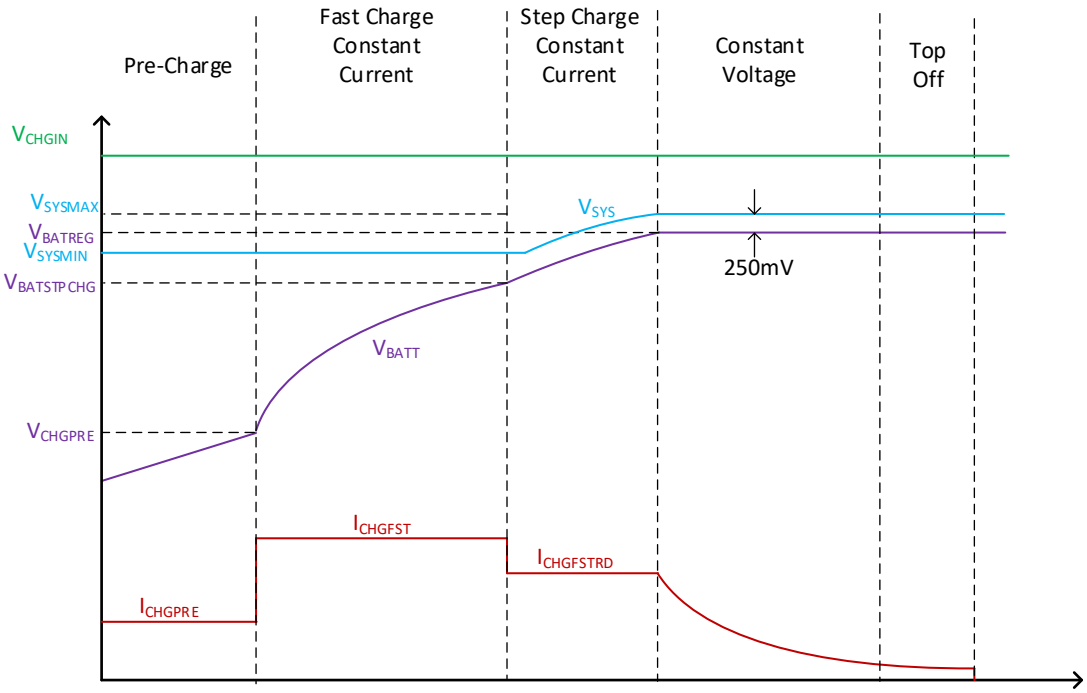


Figure 39 Charger Operation vs Temperature

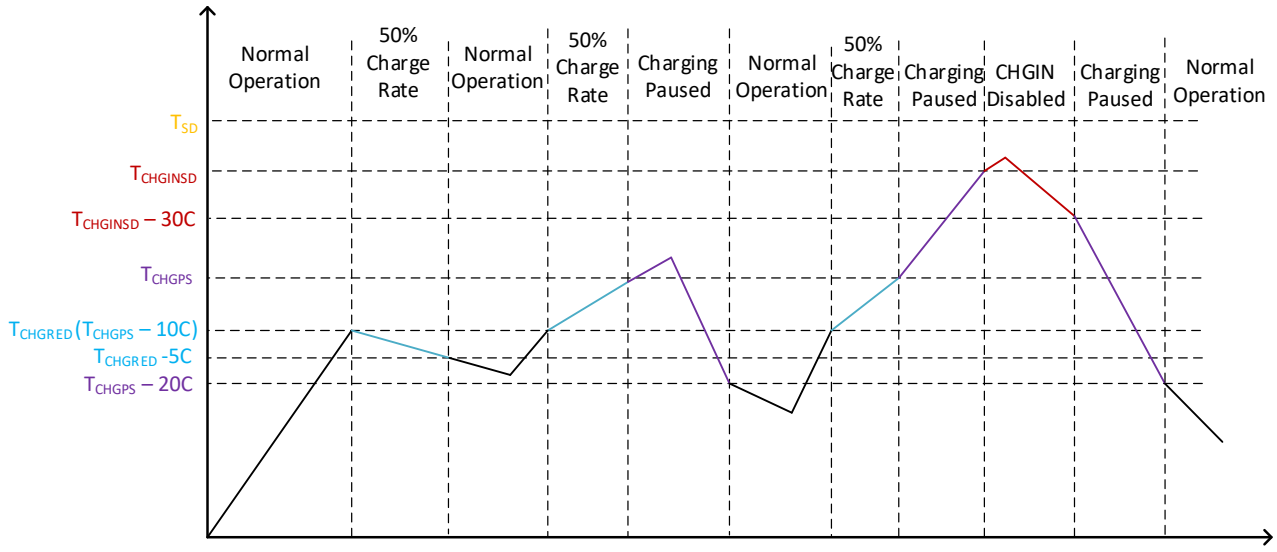
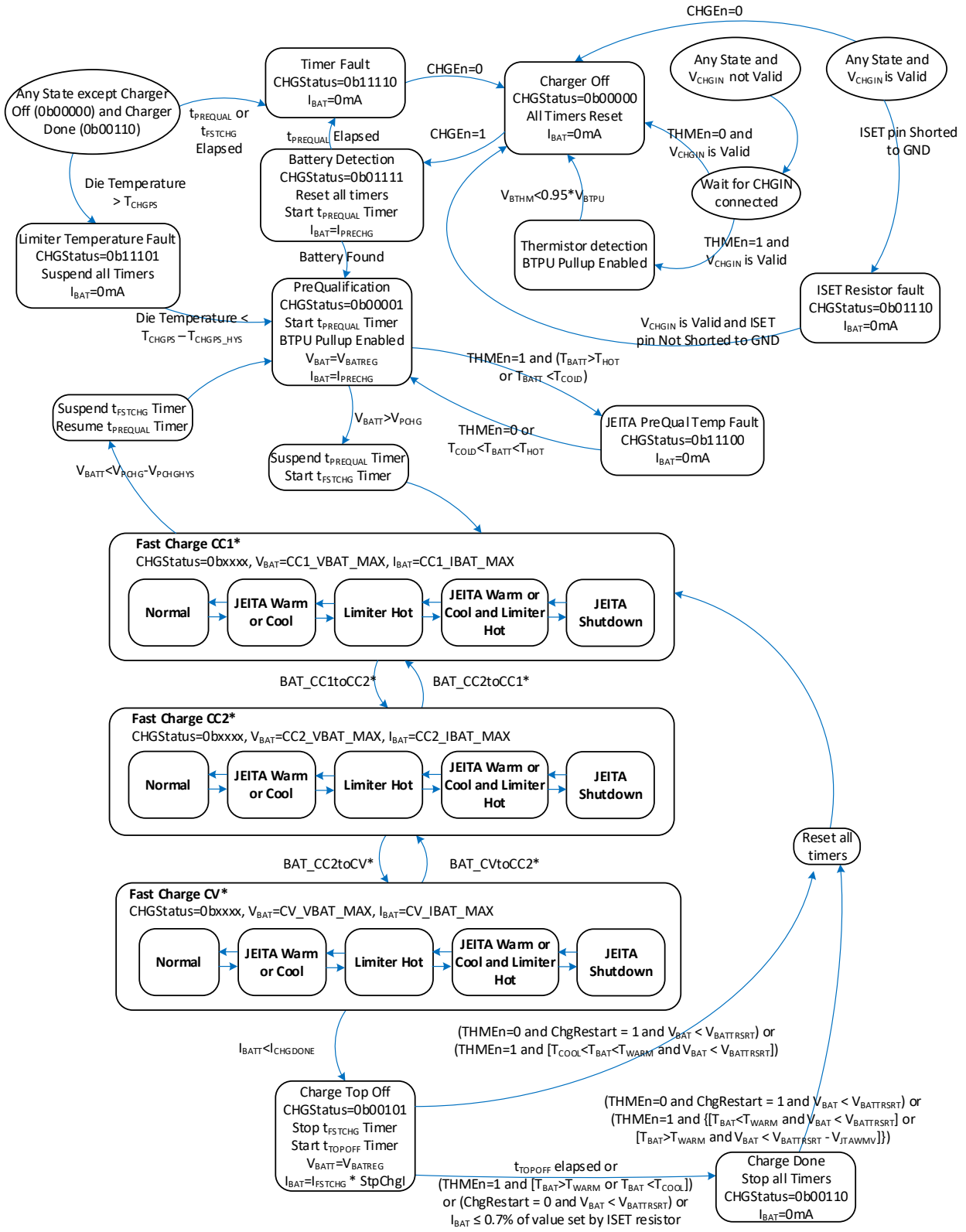


Figure 40 Li+ Charger State Diagram



*See Table 2 Charger State Diagram Substate Descriptions

Table 2 Charger State Diagram Substate Descriptions

	Normal	JEITA Warm	JEITA Cool	Limiter Hot	Limiter Hot and JEITA Warm	Limiter Hot and JEITA Cool	JEITA Shutdown
Temperature Status	$T_{COOL}<T_{BAT}<T_{WARM}$ and $T_{LIMITER}<T_{CHGRED}$	$T_{BAT}>T_{WARM}$ and $T_{LIMITER}<T_{CHGRED}$	$T_{BAT}<T_{COOL}$ and $T_{LIMITER}<T_{CHGRED}$	$T_{COOL}<T_{BAT}<T_{WARM}$ and $T_{LIMITER}>T_{CHGRED}$	$T_{BAT}>T_{WARM}$ and $T_{LIMITER}>T_{CHGRED}$	$T_{BAT}<T_{COOL}$ and $T_{LIMITER}>T_{CHGRED}$	$T_{BAT}>T_{HOT}$ or $T_{BAT}<T_{COLD}$
Timer State	Normal	Timer Doubled if JEITAWarmI=0b10 or 0b11	Timer Doubled if JEITACoolI=0b10 or 0b11	Timer Doubled	Timer Doubled	Timer Doubled	Timer Paused
BAT_CC1toCC2	$V_{BAT}\geq V_{BATREG}-V_{StepChgThs}$	$V_{BAT}\geq V_{BATREG}-V_{StepChgThs}-V_{JTAWarmV}$	$V_{BAT}\geq V_{BATREG}-V_{StepChgThs}-V_{JTACoolV}$	$V_{BAT}\geq V_{BATREG}-V_{StepChgThs}$	$V_{BAT}\geq V_{BATREG}-V_{StepChgThs}-V_{JTAWarmV}$	$V_{BAT}\geq V_{BATREG}-V_{StepChgThs}-V_{JTACoolV}$	Not Monitored
BAT_CC2toCC1	$V_{BAT}\geq V_{BATREG}-V_{StepChgThs}-V_{BATSTPHYS}$	$V_{BAT}\geq V_{BATREG}-V_{StepChgThs}-V_{JTAWarmV}-V_{BATSTPHYS}$	$V_{BAT}\geq V_{BATREG}-V_{StepChgThs}-V_{JTACoolV}-V_{BATSTPHYS}$	$V_{BAT}\geq V_{BATREG}-V_{StepChgThs}-V_{BATSTPHYS}$	$V_{BAT}\geq V_{BATREG}-V_{StepChgThs}-V_{JTAWarmV}-V_{BATSTPHYS}$	$V_{BAT}\geq V_{BATREG}-V_{StepChgThs}-V_{JTACoolV}-V_{BATSTPHYS}$	Not Monitored
BAT_CC2toCV	$V_{BAT}\geq V_{BATREG}$ and $I_{BAT}<I_{FSTCHG}$*StpChgI *FCHGRd	$V_{BAT}\geq V_{BATREG}-V_{JTAWarmV}$ and $I_{BAT}<I_{FSTCHG}$*StpChgI* JTAWarmI*FCHGRd	$V_{BAT}\geq V_{BATREG}-V_{JTACoolV}$ and $I_{BAT}<I_{FSTCHG}$*StpChgI* JTACoolI*FCHGRd	$V_{BAT}\geq V_{BATREG}$ and $I_{BAT}<I_{FSTCHG}$*StpChgI*50% *FCHGRd	$V_{BAT}\geq V_{BATREG}-V_{JTAWarmV}$ and $I_{BAT}<I_{FSTCHG}$*StpChgI* (note1) *FCHGRd	$V_{BAT}\geq V_{BATREG}-V_{JTACoolV}$ and $I_{BAT}<I_{FSTCHG}$*StpChgI* (note2) *FCHGRd	Not Monitored
BAT_CVtoCC2	$V_{BAT}<V_{BATREG}$ and $I_{BAT}\geq I_{FSTCHG}$*StpChgI *FCHGRd	$V_{BAT}<V_{BATREG}-V_{JTAWarmV}$ and $I_{BAT}\geq I_{FSTCHG}$*StpChgI* JTAWarmI*FCHGRd	$V_{BAT}<V_{BATREG}-V_{JTACoolV}$ and $I_{BAT}\geq I_{FSTCHG}$*StpChgI* JTACoolI*FCHGRd	$V_{BAT}<V_{BATREG}$ and $I_{BAT}\geq I_{FSTCHG}$*StpChgI*50% *FCHGRd	$V_{BAT}<V_{BATREG}-V_{JTAWarmV}$ and $I_{BAT}\geq I_{FSTCHG}$*StpChgI *(note1) *FCHGRd	$V_{BAT}<V_{BATREG}-V_{JTACoolV}$ and $I_{BAT}\geq I_{FSTCHG}$*StpChgI *(note2) *FCHGRd	Not Monitored
CC1_VBAT_MAX	$V_{BATREG}-V_{StepChgThs}$	$V_{BATREG}-V_{StepChgThs}-V_{JTAWarmV}$	$V_{BATREG}-V_{StepChgThs}-V_{JTACoolV}$	$V_{BATREG}-V_{StepChgThs}$	$V_{BATREG}-V_{StepChgThs}-V_{JTAWarmV}$	$V_{BATREG}-V_{StepChgThs}-V_{JTACoolV}$	0
CC1_IBAT_MAX	I_{FSTCHG}*FCHGRd	I_{FSTCHG}*JTAWarmI*FCHGRd	I_{FSTCHG}*JTACoolI*FCHGRd	I_{FSTCHG}*50%*FCHGRd	I_{FSTCHG}*(note1) *FCHGRd	I_{FSTCHG}*50%*FCHGRd	0
CC1_CHGStatus	0b00010	0x10000	0x10000	0x10001	0x10010	0x10010	0b10011
CC2_VBAT_MAX	V_{BATREG}	$V_{BATREG}-V_{JTAWarmV}$	$V_{BATREG}-V_{JTACoolV}$	V_{BATREG}	$V_{BATREG}-V_{JTAWarmV}$	$V_{BATREG}-V_{JTACoolV}$	0
CC2_IBAT_MAX	I_{FSTCHG}*StpChgI *FCHGRd	I_{FSTCHG}*StpChgI*JTAWarmI *FCHGRd	I_{FSTCHG}*StpChgI*JTACoolI *FCHGRd	I_{FSTCHG}*StpChgI*50% *FCHGRd	I_{FSTCHG}*StpChgI*(note1) *FCHGRd	I_{FSTCHG}*StpChgI*(note2) *FCHGRd	0
CC2_CHGStatus	0b00011	0x10100	0x10100	0x10101	0x10110	0x10110	0b10111
CV_VBAT_MAX	V_{BATREG}	$V_{BATREG}-V_{JTAWarmV}$	$V_{BATREG}-V_{JTACoolV}$	V_{BATREG}	$V_{BATREG}-V_{JTAWarmV}$	$V_{BATREG}-V_{JTACoolV}$	0
CV_IBAT_MAX	I_{FSTCHG}*StpChgI *FCHGRd	I_{FSTCHG}*StpChgI*JTAWarmI *FCHGRd	I_{FSTCHG}*StpChgI*JTACoolI *FCHGRd	I_{FSTCHG}*StpChgI*50% *FCHGRd	I_{FSTCHG}*StpChgI*(note1) *FCHGRd	I_{FSTCHG}*StpChgI*(note2) *FCHGRd	0
CV_CHGStatus	0b00100	0x11000	0x11000	0x11001	0x11010	0x11010	0b11011

Note1: Take the smaller of JTAWarmI or 50%

Note2: Take the smaller of JTACoolI or 50%

Thermistor Sharing

OS100X automatically uses the external thermistor connected to BTHM to measure the battery temperature for JEITA charge control. OS100X also allows the system to share the thermistor to measure system temperature. When the system would like to read the system temperature, set ThmADCEn=1. The ADC will then convert the value on BTHM as a percentage of the voltage on BTPU and make it available in the ThmADCV register. PMIC will also generate an interrupt and set the INT line low if the interrupt is unmasked. If ThmADCCn=0, the ADC converts only one new value, if another ADC value is required, the system must set ThmADCEn=0 and then write ThmADCEn=1 again to start another conversion. If ThmADCCn=1, the ADC converts continuously and stores each new value in ThmADCV. For each new value, an interrupt is generated and INT will assert low if it is unmasked.

The ADC value is calculated as V_{BTPU}/V_{BTHM} converted by an 8 bit ADC. The result is in 0.39% steps. The actual system temperature must be calculated from the Beta curve of the thermistor and the value of the resistor pullup to BTPU.

Table 3 Thermistor sharing details

THMEn	ThmADCEn	CHGIN Valid	ThmADCCn	BatPrstSt	CHGJEITASt	ThmADCV Note 3	Interrupt Generated
0	0	0	0	1	Room	00000000	No
0	1	0	0	1	Room	One new value	Yes
0	0	1	0	1	Room	00000000	No
0	1	1	0	1	Room	One new value	Yes
0	0	0	1	1	Room	00000000	No
0	1	0	1	1	Room	Continuous	Yes
0	0	1	1	1	Room	00000000	No
0	1	1	1	1	Room	Continuous	Yes
1	0	0	0	1	Room	00000000	No
1	1	0	0	1	Room	One new value	Yes
1	0	1	0	Note 1	Note 2	00000000	No
1	1	1	0	Note 1	Note 2	One new value	Yes
1	0	0	1	1	Room	00000000	No
1	1	0	1	1	Room	Continuous	Yes
1	0	1	1	Note 1	Note 2	00000000	No
1	1	1	1	Note 1	Note 2	Continuous	Yes

Note 1: 1 if ADC conversion <95% of BTPU, 0 if ADC conversion ≥95% of BTPU

Note2: Report as defined by JEITA thresholds definition.

Note 3: If ThmADCCn=0, ADC will convert one new value and stop. If ThmADCCn=1, ADC will run continuous and update ThmADCV with a new value until the ADC is disabled.

Direct Mode

Overview

This mode is intended to simplify customer testing after a device is assembled by disconnecting the battery and direct connecting CHGIN to SYS with no regulation (FETs operating as a switch). In this

mode, CHGIN will not be monitored for over or under voltage conditions and V_{SYS} must be kept between $V_{SYSUVLO}$ and 5V. The 20kohm resistor pulldown on CHGIN will be disabled to limit current drawn from CHGIN. The voltage at CHGIN must be greater than the voltage at BAT otherwise BAT will provide some of the operating current causing incorrect measurement of system current.

Sequence to enter Direct Mode

1. Set voltage at CHGIN to 5V
2. Disable charger (ChgEn=0 in register ChargeCtrl1 0x0A)
3. Turn off NTC Pullup (THMEn=0 in register ChargeCtrl2 0x0B)
4. Set Direct Mode Password (DirModePw=0xA9 in register DirectMode2 0x2B)
5. Enable Direct Mode (DirModeEn=1 in register DirectMode1 0x2A)
6. Enable charger (ChgEn=1 in register ChargeCtrl1 0x0A)
7. Decrease voltage at CHGIN to a value greater than SYSUVLO but less than the voltage connected to BAT. This is required To minimize quiescent current during in Direct Mode otherwise the internal supply selector will draw the quiescent current to run the charger from CHGIN instead of switch to draw this current from BAT.

Buck Converter

Overview

OS100X features a constant on time buck converter which balances low quiescent supply current, high efficiency, and good transient response. The buck converter requires a minimum 10uF effective bypass capacitance. The output voltage is set in 2 ranges each with 8bit resolution: 0V to 1.2V in 4.6875mV steps and 1.2V to 3.3V in 13mV steps. The buck will operate with a voltage less than 0.5V but accuracy will not be guaranteed. Both Buck1 and Buck2 can be configured to be enabled at boot up by assigning a slot in the sequencer. Assigning a startup slot will automatically enable the bucks (I2C read of Buck1Ctrl and Buck2Ctrl will be set to 0b01 in registers Buck1Ctrl1 0x12 and Buck2Ctrl1 0x18).

DVS Control

OS1000 will have 2 methods to control buck voltages for DVS: I2C and GPIO pins. In I2C mode, the buck may be set to any voltage in its programmable voltage range. If GPIO mode is used, up to 4 voltages are set corresponding to a pattern on the GPIO pins (states low/low 0b00. low/high 0b01, high/low 0b10 and high/high 0b11). The microcontroller then selects between these voltages by driving the GPIO pins. When 2 GPIO are used, the GPIO pins must transition to the new state at the same time (within <1us) or else the voltage transition time may not be clean (slope too slow or transition to a different voltage before the final value). It is important that on a microcontroller, the 2 GPIO pins are in the same bank and are set to the final value in one write to the control register and are configured for push-pull operation (not open drain since the rise and fall times are not the same).

DVS rise time is important as it defines the time the control pin must be toggled till when the microcontroller can run at full speed. OS1000 will support approximately 50mV/µs rise time with a 10uF output capacitor. DVS fall time is not as critical but the longer the voltage remains above the target set point, more energy is lost in the quiescent current of the target device. OS1000 will actively drive the voltage down to the set point by recycling the energy from the output capacitor back the input capacitor

with a fall time of approximately 2.3mV/µs only if CHGIN is not present and BAT is supplying SYS (necessary to avoid an overvoltage condition on SYS as CHGIN cannot sink current).

Enable/Disable

The buck regulators on both OS1000 and OS1001 may be enabled and disabled through I2C. In OS1000, it is also possible to enable/disable a buck regulator with a GPIO. GPIO enable/disable is the same as 1 GPIO DVS control but instead of setting a new voltage value in register BuckxVRegA, it is instead set to 0x00. Enable/Disable mode only works with 1 GPIO control (it is not possible to mix Enable/Disable and DVS modes with 2 GPIO control.

Switching Frequency adjustment

OS100X buck converters feature a constant on time design which allows adjustment of the switching frequency by varying the on time (see registers Buck1Ctrl1 0x12 and Buck2Ctrl1 0x18) approximately ±50% from the default. This may be used to move the buck operating frequency to avoid interference with sensitive components.

Alternate Operating Modes

OS100X buck converter feature 3 alternate operating modes which may be used to decrease voltage ripple at low loads or to increase efficiency at low loads (see registers Buck1Ctrl2 0x13 and Buck2Ctrl2 0x19).

Force DCM Mode

In Force DCM mode, the buck will never transition to continuous conduction mode providing a consistent ripple over a narrow operating current range. The maximum output current depends on operating conditions and programmed Ton (contact factory for full details) but typically this mode is useful for loads that are less than 50mA maximum.

Ultra High Efficiency Mode

Similar to force DCM mode, this mode forces the buck to operate in DCM mode only but turns off resources only needed for CCM mode operation thus reducing quiescent current (typically 2% or more from 100uA load to 10mA load). Ultra High Efficient Mode also limits the maximum load current that may be drawn (contact factory for full details) to less than about 10mA.

Force PWM mode

In Force PWM mode, the buck converter will always switch at a constant frequency (typically between 1.6MHz and 2.0MHz) which will result in lower efficiency especially for loads <50mA but will reduce radiated noise in the lower frequencies which can disrupt sensitive circuits in a product. It is recommended to try to fix the issue with Switching Frequency Adjustment first (see registers Buck1Ctrl1 0x12 and Buck2Ctrl1 0x18) as this does not reduce operating efficiency and only use Force PWM mode as a last resort. Force PWM may not be used with DVS.

LDO/Load Switch

LDO

The LDOs in OS100X are a low Iq design balancing transient response and noise for low current. Each LDO has a separate input supply and output pin allowing them to be used as a post converter for a buck regulator either to clean up the buck noise or to provide a lower voltage rail from a buck output to

minimize dropout voltage vs running straight from SYS. The LDO are typically controlled through I2C, but optionally a GPIO pin may be used as an enable/disable control. There is also an optional passive discharge resistor that may be enabled to discharge the output. Both LDO1 and LDO2 can be configured to be enabled at boot up by assigning a slot in the sequencer. Assigning a startup slot will automatically enable the LDOs (I2C read of LDO1Ctrl and LDO2Ctrl will be set to 0b01).

Load Switch

Each LDO may be operated in load switch mode where the voltage in the input is passed direct to the output with only resistive drop. The load switch has a 50 µs soft start to limit inrush current to charge the output capacitor.

I2C Interface

OS100X is compliant to I2C bus specification for Fast Mode (up to 1Mbit/s) according to specification UM10204 from NXP Semiconductor (www.nxp.com). Refer to this document for timing diagrams and explanation of the I2C bus and operating conditions.

I2C Bus Address read: 0x50 write:0x51

Register Map

Addr	Name	MSB	6	5	4	3	2	1	LSB
Interrupts, Status and Masks									
0x00	DeviceRev	DevId					RevId		
0x01	Status1	ChgSt					CHGINSt	CHGINOVPSt	CHGINLimSt
0x02	Status2			BatPrstSt	CHGTempFltSt	CHGTempRdSt	CHGJEITASt		
0x03	Status3			ThmADC	PSWbSt	GPIO4St	GPIO3St	GPIO2St	GPIO1St
0x04	Interrupt1					ChgStI	CHGINStI	CHGINOVPStI	CHGINLimStI
0x05	Interrupt2					BatPrstStI	CHGTempFltStI	CHGTempRdStI	CHGJEITAStI
0x06	Interrupt3			ThmADCI	PSWbStI	GPIO4StI	GPIO3StI	GPIO2StI	GPIO1StI
0x07	IntMask1					ChgStM	CHGINStM	CHGINOVPStM	CHGINLimStM
0x08	IntMask2					BatPrstStM	CHGTempFltStM	CHGTempStM	CHGJEITAStM
0x09	IntMask3			ThmADCM	PSWbStM	GPIO4StM	GPIO3StM	GPIO2StM	GPIO1StM
Charger Control									
0x0A	ChargeCtrl1	ChgEn	VCHGPre		ICHGPre		CHGInLim	CHGTempPs	
0x0B	ChargeCtrl2		THMEn	ChgRestart	StepChgIRd			ChgDone	
0x0C	ChargeCtrl3	StepChgThs							
0x0D	ChargeCtrl4	VBatReg							
0x0E	ChargeCtrl5	FCHGRd		PreQualTmr		FstChgTmr		TopOffTmr	
LDO Control									
0x0F	LDOCtrl	LDO2Mode	LDO2VRng	LDO2Ctrl		LDO1Mode	LDO1VRng	LDO1Ctrl	
0x10	LDO1Voltage	LDO1VReg							
0x11	LDO2Voltage	LDO2VReg							
Buck1 Control									
0x12	Buck1Ctrl1	Buck1ton			Buck1Ctrl		Buck1GPIO		Buck1VRng
0x13	Buck1Ctrl2							Buck1Mode	
0x14	Buck1Ctrl3	Buck1VReg							
0x15	Buck1Ctrl4	Buck1VRegA							
0x16	Buck1Ctrl5	Buck1VRegB							
0x17	Buck1Ctrl6	Buck1VRegC							
Buck2 Control									
0x18	Buck2Ctrl1	Buck2ton			Buck2Ctrl		Buck2GPIO		Buck2VRng
0x19	Buck2Ctrl2							Buck2Mode	
0x1A	Buck2Ctrl3	Buck2VReg							
0x1B	Buck2Ctrl4	Buck2VRegA							

0x1C	Buck2Ctrl5	Buck2VRegB							
0x1D	Buck2Ctrl6	Buck2VRegC							
IO Config									
0x1E	IOCfg1			GPIO2PU	GPIO2Ctrl		GPIO1PU	GPIO1Ctrl	
0x1F	IOCfg2			GPIO4PU	GPIO4Ctrl		GPIO3PU	GPIO3Ctrl	
General Configuration									
0x20	Config1	IntType		SYSUVLO		PSWbRsTm		PSWbWkTm	
0x21	Config2	Reset							ShelfMode
0x22	Config3				AddSlot	BUCK2PD	BUCK1PD	LDO2PD	LDO1PD
0x23	Config4			Buck2Slot			Buck1Slot		
0x24	Config5			LDO2Slot			LDO1Slot		
0x25	JEITAConfig1	JEITAHot							
0x26	JEITAConfig2	JEITAWarm							
0x27	JEITAConfig3	JEITACool							
0x28	JEITAConfig4	JEITACold							
0x29	JEITAConfig5	JTAWarmV		JTAWarmI		JTACoolV		JTACoolI	
Direct Mode									
0x2A	DirectMode1								DirModeEn
0x2B	DirectMode2	DirModePw							
Thermistor ADC									
0x2C	ADCConfig							ThmADCCn	ThmADCEn
0x2D	ADCValue	ThmADCV							
OTP ID									
0x2E	OTPInfo	OTPConfig							

Register Details

I2C Bus Address read: 0x50 write:0x51

DeviceRev 0x00

Bit	7	6	5	4	3	2	1	0
Name	DevId					RevId		
Read/Write	RO					RO		
Default	OTP					000		

Name	Bits	Description
DevId	7:3	Identifies OTP configuration OS1000A = 0b00000 OS1000B = 0b00001 OS1001A = 0b10001
RevId	2:0	Revision of Device Pass 1 = 0b000 Pass 2 = 0b001

Status1 0x01

Bit	7	6	5	4	3	2	1	0
Name	ChgSt					CHGINSt	CHGINOVPSt	CHGINLimSt
Read/Write	RO					RO	RO	RO
Default	00000					0	0	0

Name	Bits	Description	
ChgSt	7:3	Charger State Machine Status	
		0b00000: Charger Off	0b10000: FC_CC1 JEITA Warm/Cool
		0b00001: Prequal	0b10001: FC_CC1 Limiter Hot
		0b00010: Fast Charge CC1	0b10010: FC_CC1 JEITA Warm/Cool & Limiter Hot
		0b00011: Fast Charge CC2	0b10011: FC_CC1 JEITA Shutdown
		0b00100: Fast Charge CV	0b10100: FC_CC2 JEITA Warm/Cool
		0b00101: Charge Top Off	0b10101: FC_CC2 Limiter Hot
		0b00110: Charge Done	0b10110: FC_CC2 JEITA Warm/Cool & Limiter Hot
		0b00111: Reserved	0b10111: FC_CC2 JEITA Shutdown
		0b01000: Reserved	0b11000: FC_CV JEITA Warm/Cool
		0b01001: Reserved	0b11001: FC_CV Limiter Hot
		0b01010: Reserved	0b11010: FC_CV JEITA Warm/Cool & Limiter Hot
		0b01011: Reserved	0b11011: FC_CV JEITA Shutdown
		0b01100: Reserved	0b11100: Prequal JEITA Temp Fault
		0b01101: Reserved	0b11101: Limiter Temp Fault
		0b01110: ISET resistor fault	0b11110: Timer Fault
		0b01111: Battery Detection	0b11111: Reserved
CHGINSt	2	0: V_{CHGIN} is in the not Valid State 1: V_{CHGIN} is in the Normal or Overvoltage state See Table 1 for description of the conditions Interrupt only generated for 1 to 0 transition	
CHGINOVPSt	1	0: V_{CHGIN} is not present or is in the Normal voltage range 1: V_{CHGIN} is in the Overvoltage state See Table 1 for description of the conditions	
CHGINLimSt	0	0: Input Limiter not in thermal shutdown 1: Input limiter in thermal shutdown	

Status2 0x02

Bit	7	6	5	4	3	2	1	0
Name			BatPrstSt	CHGTempFltSt	CHGTempRdSt	CHGJEITASt		
Read/Write	RO	RO	RO	RO	RO	RO		
Default	0	0	0	0	0	0		

Name	Bits	Description
	7	Reserved
	6	Reserved
BatPrstSt	5	Battery present. Detected as an open on BTHM pin 0: Battery not present and CHGIN valid 1: Battery present or CHGIN not valid
CHGTempFltSt	4	Status of Limiter die Temperature Fault 0: Charger operating normally 1: Die temperature exceeds $T_{CHGINSD}$. Input limiter is turned off and CHGIN is disconnected from SYS
CHGTempRdSt	3	Status of charger current reduction due to die temperature. 0: Charger operating normally 1: Die temperature exceeds T_{CHGRD}, Charge current is reduced by 50% and Safety timer is doubled.
CHGJEITASt	2:0	Status of Charger JEITA temperature monitor 0b000: Cold temperature zone 0b001: Cool temperature zone 0b010: Room temperature zone 0b011: Warm temperature zone 0b100: Hot temperature zone 0b101-0b111: Reserved

Status3 0x03

Bit	7	6	5	4	3	2	1	0
Name			ThmADC	PSWbSt	GPIO4St	GPIO3St	GPIO2St	GPIO1St
Read/Write	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Name	Bits	Description
	7:6	Reserved
ThmADC	5	Status of Thermistor ADC conversion complete. Only valid when ThmADCEn=1. 0: ADC conversion in progress 1: ADC conversion complete
PSWbSt	4	Status of PSWb. 0: PSWb state is low 1: PSWb state is high
GPIO4St	3	Status of GPIO4 pin. (Valid only when configured for GPIO input mode) 0: GPIO4 state is low 1: GPIO4 state is high
GPIO3St	2	Status of GPIO3 pin. (Valid only when configured for GPIO input mode) 0: GPIO3 state is low 1: GPIO3 state is high
GPIO2St	1	Status of GPIO2 pin. (Valid only when configured for GPIO input mode) 0: GPIO2 state is low 1: GPIO2 state is high
GPIO1St	0	Status of GPIO1 pin. (Valid only when configured for GPIO input mode) 0: GPIO1 state is low 1: GPIO1 state is high

Interrupt1 0x04

Bit	7	6	5	4	3	2	1	0
Name					ChgStI	CHGINStI	CHGINOVPStI	CHGINLimStI
Read/Write					RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Register cleared upon Read

Name	Bits	Description
	7:4	Reserved
ChgStI	3	Interrupt for change in Charger Status 0: No Change 1: Status Change
CHGINStI	2	Interrupt for change in CHGIN voltage Status. 0: No Change 1: Status Change
CHGINOVPStI	1	Interrupt for change in CHGIN OVP Status 0: No Change 1: Status Change
CHGINLimStI	0	Interrupt for change in CHGIN Thermal Status 0: No Change 1: Status Change

Interrupt2 0x05

Bit	7	6	5	4	3	2	1	0
Name					BatPrstStI	CHGTempFltStI	CHGTempRdStI	CHGJEITAStI
Read/Write	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Register cleared upon Read

Name	Bits	Description
	7:4	Reserved
BatPrstStI	3	Interrupt for change in Battery Present Status 0: No Change 1: Status Change
CHGTempFltStI	2	Interrupt for change in Charger Temperature Fault Status 0: No Change 1: Status Change
CHGTempRdStI	1	Interrupt for change in Charger Temperature Pause Status 0: No Change 1: Status Change
CHGJEITAStI	0	Interrupt for change in Charger JEITA Monitor Status 0: No Change 1: Status Change

Interrupt3 0x06

Bit	7	6	5	4	3	2	1	0
Name			ThmADCI	PSWbStI	GPIO4StI	GPIO3StI	GPIO2StI	GPIO1StI
Read/Write	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Register cleared upon Read

Name	Bits	Description
	7:6	Reserved
ThmADCI	5	Interrupt for change in ThmADC Status. 0: No Change 1: Status Change
PSWbStI	4	Interrupt for change in PSWb Status 0: No Change 1: Status Change
GPIO4StI	3	Interrupt for change in GPIO4 Status 0: No Change 1: Status Change
GPIO3StI	2	Interrupt for change in GPIO3 Status 0: No Change 1: Status Change
GPIO2StI	1	Interrupt for change in GPIO2 Status 0: No Change 1: Status Change
GPIO1StI	0	Interrupt for change in GPIO1 Status 0: No Change 1: Status Change

IntMask1 0x07

Bit	7	6	5	4	3	2	1	0
Name					ChgStM	CHGINStM	CHGINOVPStM	CHGINLimStM
Read/Write					R/W	R/W	R/W	R/W
Default	0	0	0	0	1	1	1	1

Name	Bits	Description
	7:4	Reserved
ChgStM	3	Interrupt Mask for change in Charger Status 0: No Mask 1: Mask Interrupt Contribution to INT pin
CHGINStM	2	Interrupt Mask for change in CHGIN voltage Status 0: No Mask 1: Mask Interrupt Contribution to INT pin
CHGINOVPStM	1	Interrupt Mask for change in CHGIN OVP Status 0: No Mask 1: Mask Interrupt Contribution to INT pin
CHGINLimStM	0	Interrupt Mask for change in CHGIN Thermal Status 0: No Mask 1: Mask Interrupt Contribution to INT pin

IntMask2 0x08

Bit	7	6	5	4	3	2	1	0
Name					BatPrstStM	CHGTempFltStM	CHGTempStM	CHGJEITAStM
Read/Write	RO	RO	RO	RO	R/W	R/W	R/W	R/W
Default	0	0	0	0	1	1	1	1

Name	Bits	Description
	7:4	Reserved
BatPrstStM	3	Interrupt Mask for change in Battery Present Status 0: No Mask 1: Mask Interrupt Contribution to INT pin
CHGTempFltStM	2	Interrupt Mask for change in Charger Temperature Fault Status 0: No Mask 1: Mask Interrupt Contribution to INT pin
CHGTempRdStM	1	Interrupt Mask for change in Charger Temperature Pause Status 0: No Mask 1: Mask Interrupt Contribution to INT pin
CHGJEITAStM	0	Interrupt Mask for change in Charger JEITA Monitor Status 0: No Mask 1: Mask Interrupt Contribution to INT pin

IntMask3 0x09

Bit	7	6	5	4	3	2	1	0
Name			ThmADCM	PSWbStM	GPIO4StM	GPIO3StM	GPIO2StM	GPIO1StM
Read/Write	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	1	1	1	1	1	1

Name	Bits	Description
	7:6	Reserved
ThmADCM	5	Interrupt Mask for change in PSWb Status. Interrupt Mask for change in PSWb Status 0: No Mask 1: Mask Interrupt Contribution to INT pin
PSWbStM	4	Interrupt Mask for change in PSWb Status 0: No Mask 1: Mask Interrupt Contribution to INT pin
GPIO4StM	3	Interrupt Mask for change in GPIO4 Status 0: No Mask 1: Mask Interrupt Contribution to INT pin
GPIO3StM	2	Interrupt Mask for change in GPIO3 Status 0: No Mask 1: Mask Interrupt Contribution to INT pin
GPIO2StM	1	Interrupt Mask for change in GPIO2 Status 0: No Mask 1: Mask Interrupt Contribution to INT pin
GPIO1StM	0	Interrupt Mask for change in GPIO1 Status 0: No Mask 1: Mask Interrupt Contribution to INT pin

ChargeCtrl1 0x0A

Bit	7	6	5	4	3	2	1	0
Name	ChgEn	VCHGPre		ICHGPre		CHGInLim	CHGTempPs	
Read/Write	R/W	R/W		R/W		R/W	R/W	
Default	OTP	OTP		OTP		OTP	OTP	

Name	Bits	Description
ChgEn	7	Enable Battery Charger. 0: Disabled 1: Enabled
VCHGPre	6:5	Pre-Charge Voltage Threshold 0b00: 2.1V 0b01: 2.4V 0b10: 2.7V 0b11: 3.0V
ICHGPre	4:3	Pre-Charge Current 0b00: 3.125% 0b01: 6.25% 0b10: 12.5% 0b11: 25%
CHGInLim	2	Input Current Limit 0: 450mA 1: 1000mA
CHGTempPs	1:0	Temperature where charger pauses due to increasing die temperature. 0b00: 60°C 0b01: 80°C 0b10: 100°C 0b11: 120°C

ChargeCtrl2 0x0B

Bit	7	6	5	4	3	2	1	0
Name		THMEn	ChgRestart	StepChgIRd			ChgDone	
Read/Write	RO	R/W	R/W	R/W			R/W	
Default	0	OTP	OTP	OTP			OTP	

Name	Bits	Description
	7	Reserved
THMEn	6	Enable Battery Thermistor monitor 0: Disabled 1: Enabled
ChgRestart	5	Charger auto restart after drop in voltage 0: No restart 1: Auto restart after V_{BATT} drops by $V_{BATTRSRT}$
StepChgIRd	4:2	Step Charge Current Reduction in % of I_{CHGFST} 0b000: 50% 0b001: 60% 0b010: 70% 0b011: 80% 0b100: 85% 0b101: 90% 0b110: 95% 0b111: 100%
CHGDone	1:0	Current threshold in % of I_{CHGFST} where charging is declared complete. 0b00: 2.5% 0b01: 5% 0b10: 10% 0b11: 20%

ChargeCtrl3 0x0C

Bit	7	6	5	4	3	2	1	0
Name	StepChgThs							
Read/Write	R/W							
Default	OTP							

Name	Bits	Description
StepChgThs	7:0	Step Charge voltage threshold in 4.6875mV steps. $V_{BATSTPCHG}$=((value+1)*4.6875mV)+3.6V. Writing a value greater than 0b11011111 (0xDF) will be held at 4.65V. StepChgThs must be set to a value less than or equal to VBatReg.

ChargeCtrl4 0x0D

Bit	7	6	5	4	3	2	1	0
Name	VBatReg							
Read/Write	R/W							
Default	OTP							

Name	Bits	Description
VBatReg	7:0	Battery regulation voltage in CV mode in 4.6875mV steps. V_{BATREG}=((value+1)*4.6875mV)+3.6V. Writing a value greater than 0b11011111 (0xDF) will be held at 4.65V. VBatReg must be set to a value greater than or equal to StepChgThs.

ChargeCtrl5 0x0E

Bit	7	6	5	4	3	2	1	0
Name	FCHGRd		PreQualTmr		FstChgTmr		TopOffTmr	
Read/Write	R/W		R/W		R/W		R/W	
Default	00		OTP		OTP		OTP	

Name	Bits	Description
FCHGRd	7:6	Reduction in Maximum charge current defined by resistor on ISET pin 0b00: 100% 0b01: 50% 0b10: 25% 0b11: 12.5%
PreQualTmr	5:4	Maximum time allowed for charger in prequalification mode 0b00: 30 min 0b01: 60 min 0b10: 90 min 0b11: 120 min
FstChgTmr	3:2	Maximum time allowed for charger in fast charge mode 0b00: 1.5 hours 0b01: 4 hours 0b10: 6.5 hours 0b11: 9 hours
TopOffTmr	1:0	Maximum time allowed for charger in top off 0b00: 0 min 0b01: 10 min 0b10: 20 min 0b11: 30 min

LDOCtrl 0x0F

Bit	7	6	5	4	3	2	1	0
Name	LDO2Mode	LDO2VRng	LDO2Ctrl		LDO1Mode	LDO1VRng	LDO1Ctrl	
Read/Write	R/W	R/W	R/W		R/W	R/W	R/W	
Default	OTP	OTP	00*		OTP	OTP	00*	

* Default will be 0b01 if the LDO is assigned a slot in the sequencer by OTP.

Name	Bits	Description
LDO2Mode	7	Set either LDO mode or Load Switch mode. 0: LDO mode 1: Load switch mode
LDO2VRng	6	Set Output voltage range for LDO2. **Disable regulator before changing the output range.** 0: 0V to 1.2V 1: 0V to 3.3V
LDO2Ctrl	5:4	Enable/disable by I2C or GPIO control. If 0b10 or 0b11 selected but GPIO pin mode not also changed to LDO/Buck control, LDO will be default disabled. 0b00: Disable 0b01: Enable 0b10: GPIO3 control 0b11: GPIO4 control
LDO1Mode	3	Set either LDO mode or Load Switch mode. 0: LDO mode 1: Load switch mode
LDO1VRng	2	Set Output voltage range for LDO1. **Disable regulator before changing the output range.** 0: 0V to 1.2V 1: 0V to 3.3V
LDO1Ctrl	1:0	Enable/disable by I2C or GPIO control. If 0b10 or 0b11 selected but GPIO pin mode not also changed to LDO/Buck control, LDO will be default disabled. 0b00: Disable 0b01: Enable 0b10: GPIO3 control 0b11: GPIO4 control

LDO1Voltage 0x10

Bit	7	6	5	4	3	2	1	0
Name	LDO1VReg							
Read/Write	R/W							
Default	OTP							

Name	Bits	Description
LDO1VReg	7:0	Set output voltage of LDO1. LDO1VRng=0: V_{LDO1}=(1+value)*0.004687. Specs are guaranteed above 0.5V LDO1VRng=1: V_{LDO1}=(1+value)*0.01289. Specs are guaranteed above 1.3V

LDO2Voltage 0x11

Bit	7	6	5	4	3	2	1	0
Name	LDO2VReg							
Read/Write	R/W							
Default	OTP							

Name	Bits	Description
LDO2VReg	7:0	Set output voltage of LDO2. LDO2VRng=0: V_{LDO2}=(1+value)*0.004687. Specs are guaranteed above 0.5V LDO2VRng=1: V_{LDO2}=(1+value)*0.01289. Specs are guaranteed above 1.3V

Buck1Ctrl1 0x12

Bit	7	6	5	4	3	2	1	0
Name	Buck1ton			Buck1Ctrl		Buck1GPIO		Buck1VRng
Read/Write	R/W			R/W		R/W		R/W
Default	OTP			00*		00		OTP

* Default will be 0b01 if the Buck is assigned a slot in the sequencer by OTP.

Name	Bits	Description
Buck1ton	7:5	Adjust Buck1 converter on time to adjust operation frequency. 0b000: -52% 0b001: -35% 0b010: -18% 0b011: 0% 0b100: 18% 0b101: 35% 0b110: 52% 0b111: 68%
Buck1Ctrl	4:3	Enable/disable by I2C or GPIO control. If a GPIO mode selected but GPIO pin/pins mode not also changed to LDO/Buck control, Buck will be default disabled. 0b00: Disable 0b01: Enable 0b10: OS1000 - GPIO control (see Buck1GPIO for details) OS1001 - Disable 0b11: OS1000 - Reserved OS1001 - Enable
Buck1GPIO	2:1	GPIO control mode. If a GPIO mode selected but GPIO pin/pins mode not also changed to LDO/Buck control, Buck will be default disabled. (OS1000 only) 0b00: GPIO3 control (switch between 2 different voltages) 0b01: GPIO4 control (switch between 2 different voltages) 0b10: GPIO3 and GPIO4 control (switch between 4 different voltages) 0b11: Reserved
Buck1VRng	0	Set Output voltage range for Buck1. **Disable regulator before changing the output range.** 0: 0V to 1.2V 1: 0V to 3.3V

Buck1Ctrl2 0x13

Bit	7	6	5	4	3	2	1	0
Name							Buck1Mode	
Read/Write	RO	RO	RO	RO	RO	RO	R/W	
Default	0	0	0	0	0	0	00	

Name	Bits	Description
	7:2	Reserved
Buck1Mode	1:0	Buck1 Operating Mode. 0b00: Normal 0b01: Force DCM. 0b10: Ultra High Efficiency Mode. 0b11: Force PWM

Buck1Ctrl3 0x14

Bit	7	6	5	4	3	2	1	0
Name	Buck1VReg							
Read/Write	R/W							
Default	OTP							

Name	Bits	Description
Buck1VReg	7:0	Buck1 Output voltage. Voltage set if: Buck1Ctrl=0b01 or Buck1Ctrl=0b10 and Buck1GPIO=0b00 and GPIO3=low or Buck1Ctrl=0b10 and Buck1GPIO=0b01 and GPIO4=low or Buck1Ctrl=0b10 and Buck1GPIO=0b10 and GPIO4/3=low/low.
		Buck1VRng=0: V_{BUCK1}= (1+value)*0.0046875. Specifications are guaranteed above 0.5V Buck1VRng=1: V_{BUCK1}=(1+value)*0.0129. Specifications are guaranteed above 1.2V

Buck1Ctrl4 0x15

Bit	7	6	5	4	3	2	1	0
Name	Buck1VRegA							
Read/Write	R/W							
Default	00000000							

Name	Bits	Description
Buck1VRegA	7:0	Buck1 Output voltage. Voltage set if: Buck1Ctrl=0b10 and Buck1GPIO=0b00 and GPIO3=high or Buck1Ctrl=0b10 and Buck1GPIO=0b01 and GPIO4=high or Buck1Ctrl=0b10 and Buck1GPIO=0b10 and GPIO4/3=low/high.
		Buck1VRng=0: V_{BUCK1}= (1+value)*0.0046875. Specifications are guaranteed above 0.5V Buck1VRng=1: V_{BUCK1}= (1+value)*0.0129. Specifications are guaranteed above 1.2V

Buck1Ctrl5 0x16

Bit	7	6	5	4	3	2	1	0
Name	Buck1VRegB							
Read/Write	R/W							
Default	00000000							

Name	Bits	Description
Buck1VRegB	7:0	Buck1 Output voltage. Voltage set if Buck1Ctrl=0b10 and Buck1GPIO=0b10 and GPIO4/3=high/low.
		Buck1VRng=0: V_{BUCK1}=(1+value)*0.0046875. Specifications are guaranteed above 0.5V Buck1VRng=1: V_{BUCK1}= (1+value)*0.0129. Specifications are guaranteed above 1.2V

Buck1Ctrl6 0x17

Bit	7	6	5	4	3	2	1	0
Name	Buck1VRegC							
Read/Write	R/W							
Default	00000000							

Name	Bits	Description
Buck1VRegC	7:0	Buck1 Output voltage. Voltage set if Buck1Ctrl=0b10 and Buck1GPIO=0b10 and GPIO4/3=high/high.
		Buck1VRng=0: V_{BUCK1}=(1+value)*0.0046875. Specifications are guaranteed above 0.5V Buck1VRng=1: V_{BUCK1}= (1+value)*0.0129. Specifications are guaranteed above 1.2V

Buck2Ctrl1 0x18

Bit	7	6	5	4	3	2	1	0
Name	Buck2ton			Buck2Ctrl		Buck2GPIO		Buck2VRng
Read/Write	R/W			R/W		R/W		R/W
Default	OTP			00*		00		OTP

* Default will be 0b01 if the Buck is assigned a slot in the sequencer by OTP.

Name	Bits	Description
Buck2ton	7:5	Adjust Buck2 converter on time to adjust operation frequency. 0b000: -52% 0b001: -35% 0b010: -18% 0b011: 0% 0b100: 18% 0b101: 35% 0b110: 52% 0b111: 68%
Buck2Ctrl	4:3	Enable/disable by I2C or GPIO control. If a GPIO mode selected but GPIO pin/pins mode not also changed to LDO/Buck control, Buck will be default disabled. 0b00: Disable 0b01: Enable 0b10: OS1000 - GPIO control (see Buck1GPIO for details) OS1001 - Disable 0b11: OS1000 - Reserved OS1001 - Enable
Buck2GPIO	2:1	GPIO control mode. If a GPIO mode selected but GPIO pin/pins mode not also changed to LDO/Buck control, Buck will be default disabled. (OS1000 only) 0b00: GPIO3 control (switch between 2 different voltages) 0b01: GPIO4 control (switch between 2 different voltages) 0b10: GPIO3 and GPIO4 control (switch between 4 different voltages) 0b11: Reserved
Buck2VRng	0	Set Output voltage range for Buck2. **Disable regulator before changing the output range.** 0: 0V to 1.2V 1: 0V to 3.3V

Buck2Ctrl2 0x19

Bit	7	6	5	4	3	2	1	0
Name							Buck2Mode	
Read/Write	RO	RO	RO	RO	RO	RO	R/W	
Default	0	0	0	0	0	0	00	

Name	Bits	Description
	7:2	Reserved
Buck2Mode	1:0	Buck2 Operating Mode. 0b00: Normal 0b01: Force DCM. 0b10: Ultra High Efficiency Mode. 0b11: Force PWM

Buck2Ctrl3 0x1A

Bit	7	6	5	4	3	2	1	0
Name	Buck2VReg							
Read/Write	R/W							
Default	OTP							

Name	Bits	Description
Buck2VReg	7:0	Buck2 Output voltage. Voltage set if: Buck2Ctrl=0b01 or Buck2Ctrl=0b10 and Buck2GPIO=0b00 and GPIO3=low or Buck2Ctrl=0b10 and Buck2GPIO=0b01 and GPIO4=low or Buck2Ctrl=0b10 and Buck2GPIO=0b10 and GPIO4/3=low/low.
		Buck2VRng=0: V_{BUCK2}= (1+value)*0.0046875. Specifications are guaranteed above 0.5V Buck2VRng=1: V_{BUCK2}= (1+value)*0.0129. Specifications are guaranteed above 1.2V

Buck2Ctrl4 0x1B

Bit	7	6	5	4	3	2	1	0
Name	Buck2VRegA							
Read/Write	R/W							
Default	00000000							

Name	Bits	Description
Buck2VRegA	7:0	Buck2 Output voltage. Voltage set if: Buck2Ctrl=0b10 and Buck2GPIO=0b00 and GPIO3=high or Buck2Ctrl=0b10 and Buck2GPIO=0b01 and GPIO4=high or Buck2Ctrl=0b10 and Buck2GPIO=0b10 and GPIO4/3=low/high.
		Buck2VRng=0: V_{BUCK2}=(1+value)*0.0046875. Specifications are guaranteed above 0.5V Buck2VRng=1: V_{BUCK2}= (1+value)*0.0129. Specifications are guaranteed above 1.2V

Buck2Ctrl5 0x1C

Bit	7	6	5	4	3	2	1	0
Name	Buck2VRegB							
Read/Write	R/W							
Default	00000000							

Name	Bits	Description
Buck2VRegB	7:0	Buck2 Output voltage. Voltage set if Buck2Ctrl=0b10 and Buck2GPIO=0b10 and GPIO4/3=high/low.
		Buck2VRng=0: V_{BUCK2}= (1+value)*0.0046875. Specifications are guaranteed above 0.5V Buck2VRng=1: V_{BUCK2}= (1+value)*0.0129. Specifications are guaranteed above 1.2V

Buck2Ctrl6 0x1D

Bit	7	6	5	4	3	2	1	0
Name	Buck2VRegC							
Read/Write	R/W							
Default	00000000							

Name	Bits	Description
Buck2VRegC	7:0	Buck2 Output voltage. Voltage set if Buck2Ctrl=0b10 and Buck2GPIO=0b10 and GPIO4/3=high/high.
		Buck2VRng=0: V_{BUCK2}=(1+value)*0.0046875. Specifications are guaranteed above 0.5V Buck2VRng=1: V_{BUCK2}= (1+value)*0.0129. Specifications are guaranteed above 1.2V

IOCfg1 0x1E

Bit	7	6	5	4	3	2	1	0
Name			GPIO2PU	GPIO2Ctrl		GPIO1PU	GPIO1Ctrl	
Read/Write	RO	RO	R/W	R/W		R/W	R/W	
Default	0	0	OTP	OTP		OTP	OTP	

Name	Bits	Description
	7	Reserved
	6	Reserved
GPIO2PU	5	Pullup to VIO enabled on GPIO2 (independent of GPIO set to input, push/pull or open drain modes) 0: Pullup disabled 1: pullup enabled
GPIO2Ctrl	4:3	GPIO2 Control 0b00: General purpose Input (status in register 0x03) 0b01: Drive Low 0b10: Drive high 0b11: Open Drain reset output – asserted during power up sequencing
GPIO1PU	2	Pullup to VIO enabled on GPIO1 (independent of GPIO set to input, push/pull or open drain modes) 0: Pullup disabled 1: pullup enabled
GPIO1Ctrl	1:0	GPIO1 Control 0b00: General purpose Input (status in register 0x03) 0b01: Drive Low 0b10: Drive high 0b11: Open Drain output follows state of PSWB input

IOCfg2 0x1F

Bit	7	6	5	4	3	2	1	0
Name			GPIO4PU	GPIO4Ctrl		GPIO3PU	GPIO3Ctrl	
Read/Write	RO	RO	R/W	R/W		R/W	R/W	
Default	0	0	OTP	OTP		OTP	OTP	

Name	Bits	Description
	7	Reserved
	6	Reserved
GPIO4PU	5	Pullup to VIO enabled on GPIO4 (independent of GPIO set to input, push/pull or open drain modes) 0: Pullup disabled 1: pullup enabled
GPIO4Ctrl	4:3	GPIO4 Control 0b00: General purpose Input (status in register 0x03) 0b01: Drive Low 0b10: Drive high 0b11: OS1000 - LDO/Buck control OS1001 – LDO control
GPIO3PU	2	Pullup to VIO enabled on GPIO3 (independent of GPIO set to input, push/pull or open drain modes) 0: Pullup disabled 1: pullup enabled
GPIO3Ctrl	1:0	GPIO3 Control 0b00: General purpose Input (status in register 0x03) 0b01: Drive Low 0b10: Drive high 0b11: OS1000 - LDO/Buck control OS1001 – LDO control

Config1 0x20

Bit	7	6	5	4	3	2	1	0
Name	IntType		SYSUVLO		PSWbRsTm		PSWbWkTm	
Read/Write	R/W		R/W		R/W		R/W	
Default	00		OTP		OTP		OTP	

Name	Bits	Description
IntType	7:6	Interrupt Enable and Type. 0b00: Interrupt Disabled. 0b01: Interrupt enabled with level trigger (idle high, drive low). 0b10: Interrupt enabled with pulse trigger (500us low on INT). 0b11: Reserved
SYSUVLO	5:4	UVLO Threshold where OS100X turns off and returns to shelf mode (CHGIN not valid) or resets and restarts (CHGIN valid). 0b00: 2.7V 0b01: 2.9V 0b10: 3.0V 0b11: 3.2V
PSWbRsTm	3:2	PSWb reset time. Time that PSWb must be pulled low to reset all registers in OS100X to default. 0b00: Disabled 0b01: 5s 0b10: 9s 0b11: 12s
PSWbWkTm	1:0	PSWb wake time. Time that PSWb must be pulled low to wake from Shelf Mode 0b00: Disabled 0b01: 500ms 0b10: 1000ms 0b11: 2000ms

Config2 0x21

Bit	7	6	5	4	3	2	1	0
Name	Reset							ShelfMode
Read/Write	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Name	Bits	Description
Reset	7	Chip reset request. All registers reset to defaults after 1ms and restart of regulators. 0: Normal operation 1: PMIC Reset
	6:1	Reserved
ShelfMode	0	Enter Shelf Mode. SYS and all functions will be disabled 0: Normal operation 1: Enter Shelf Mode

Config3 0x22

Bit	7	6	5	4	3	2	1	0
Name				AddSlot	BUCK2PD	BUCK1PD	LDO2PD	LDO1PD
Read/Write	RO	RO	RO	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	OTP	OTP	OTP	OTP	OTP

Name	Bits	Description
	7:5	Reserved
AddSlot	4	Add an additional slot at the end of the startup sequence 0: Disabled 1: Enabled
BUCK2PD	3	Enable Passive pull down when BUCK2 is disabled. 0: Disabled 1: Enabled
BUCK1PD	2	Enable Passive pull down when BUCK1 is disabled. 0: Disabled 1: Enabled
LDO2PD	1	Enable Passive pull down when LDO2 is disabled. 0: Disabled 1: Enabled
LDO1PD	0	Enable Passive pull down when LDO1 is disabled. 0: Disabled 1: Enabled

Config4 0x23

Bit	7	6	5	4	3	2	1	0
Name			Buck2Slot			Buck1Slot		
Read/Write	RO	RO	R/W			R/W		
Default	0	0	OTP			OTP		

Name	Bits	Description
	7:6	Reserved
Buck2Slot	5:3	Enable Slot for Buck2. Setting a value other than 0b000 will auto set the bits Buck2Ctrl to 0b01 0b000: Regulator not powered up by default 0b001: Slot1 0b010: Slot2 0b011: Slot3 0b1xx: Slot4
Buck1Slot	2:0	Enable Slot for Buck1. Setting a value other than 0b000 will auto set the bits Buck1Ctrl to 0b01 0b000: Regulator not powered up by default 0b001: Slot1 0b010: Slot2 0b011: Slot3 0b1xx: Slot4

Config5 0x24

Bit	7	6	5	4	3	2	1	0
Name			LDO2Slot			LDO1Slot		
Read/Write	RO	RO	R/W			R/W		
Default	0	0	OTP			OTP		

Name	Bits	Description
	7:6	Reserved
LDO2Slot	5:3	Enable Slot for LDO2. Setting a value other than 0b000 will auto set the bits LDO2Ctrl to 0b01 0b000: Regulator not powered up by default 0b001: Slot1 0b010: Slot2 0b011: Slot3 0b1xx: Slot4
LDO1Slot	2:0	Enable Slot for LDO1. Setting a value other than 0b000 will auto set the bits LDO1Ctrl to 0b01 0b000: Regulator not powered up by default 0b001: Slot1 0b010: Slot2 0b011: Slot3 0b1xx: Slot4

JEITAConfig1 0x25

Bit	7	6	5	4	3	2	1	0
Name	JEITAHot							
Read/Write	R/W							
Default	OTP							

Name	Bits	Description
JEITAHot	7:0	Threshold for JEITA Hot Temperature. Set as a percentage of pullup voltage at BTPU pin. 256 values in 0.392% steps 0b00000000: 0% 0b00000001: 0.39% 0b00000010: 0.78% … 0b11111111: 100%

JEITAConfig2 0x26

Bit	7	6	5	4	3	2	1	0
Name	JEITAWarm							
Read/Write	R/W							
Default	OTP							

Name	Bits	Description
JEITAWarm	7:0	Threshold for JEITA Warm Temperature. Set as a percentage of pullup voltage at BTPU pin. 256 values in 0.392% steps 0b00000000: 0% 0b00000001: 0.39% 0b00000010: 0.78% … 0b11111111: 100%

JEITAConfig3 0x27

Bit	7	6	5	4	3	2	1	0
Name	JEITACool							
Read/Write	R/W							
Default	OTP							

Name	Bits	Description
JEITACool	7:0	Threshold for JEITA Cool Temperature. Set as a percentage of pullup voltage at BTPU pin. 256 values in 0.392% steps 0b00000000: 0% 0b00000001: 0.39% 0b00000010: 0.78% … 0b11111111: 100%

JEITAConfig4 0x28

Bit	7	6	5	4	3	2	1	0
Name	JEITACold							
Read/Write	R/W							
Default	OTP							

Name	Bits	Description
JEITACold	7:0	Threshold for JEITA Cold Temperature. Set as a percentage of pullup voltage at BTPU pin. 256 values in 0.392% steps 0b00000000: 0% 0b00000001: 0.39% 0b00000010: 0.78% … 0b11111111: 100%

JEITAConfig5 0x29

Bit	7	6	5	4	3	2	1	0
Name	JTAWarmV		JTAWarmI		JTACoolV		JTACoolI	
Read/Write	R/W		R/W		R/W		R/W	
Default	OTP		OTP		OTP		OTP	

Name	Bits	Description
JTAWarmV	7:6	JEITA warm temperature battery voltage reduction 0b00: 0V 0b01: 50mV 0b10: 150mV 0b11: 250mV
JTAWarmI	5:4	JEITA warm temperature battery current reduction 0b00: Disabled 0b10: 12.5% 0b11: 25% 0b11: 50%
JTACoolV	3:2	JEITA cool temperature battery voltage reduction 0b00: 0V 0b01: 50mV 0b10: 150mV 0b11: 250mV
JTACoolI	1:0	JEITA cool temperature battery current reduction 0b00: Disabled 0b10: 12.5% 0b11: 25% 0b11: 50%

DirectMode1 0x2A

Bit	7	6	5	4	3	2	1	0
Name								DirModeEn
Read/Write	RO	RO	RO	RO	RO	RO	RO	R/W
Default	0	0	0	0	0	0	0	0

Name	Bits	Description
	7:1	Reserved
DirModeEn	0	Enable Direct Mode. 0: Disabled 1: Enabled

DirectMode2 0x2B

Bit	7	6	5	4	3	2	1	0
Name	DirModePw							
Read/Write	R/W							
Default	00000000							

Name	Bits	Description
DirModePw	7:0	Password to enable Direct Mode. Write this value to 0xA9 before setting DirModeEn=1 to enable direct mode.

ADCConfig 0x2C

Bit	7	6	5	4	3	2	1	0
Name							ThmADCCn	ThmADCEn
Read/Write	RO	RO	RO	RO	RO	RO	R/W	R/W
Default	0	0	0	0	0	0	0	0

Name	Bits	Description
	7:2	Reserved
ThmADCCn	1	Thermistor ADC continuous conversion. (note that this causes increases current consumption when operating on battery) 0: One Shot mode 1: Continuous
ThmADCEn	0	Enable Thermistor ADC. 0: Disabled 1: Enabled

ADCValue 0x2D

Bit	7	6	5	4	3	2	1	0
Name	ThmADCV							
Read/Write	RO							
Default	00000000							

Name	Bits	Description
ThmADCV	7:0	Output value from Thermistor ADC. Value is a percentage of pullup voltage at BTPU pin. 256 values in 0.39% steps.

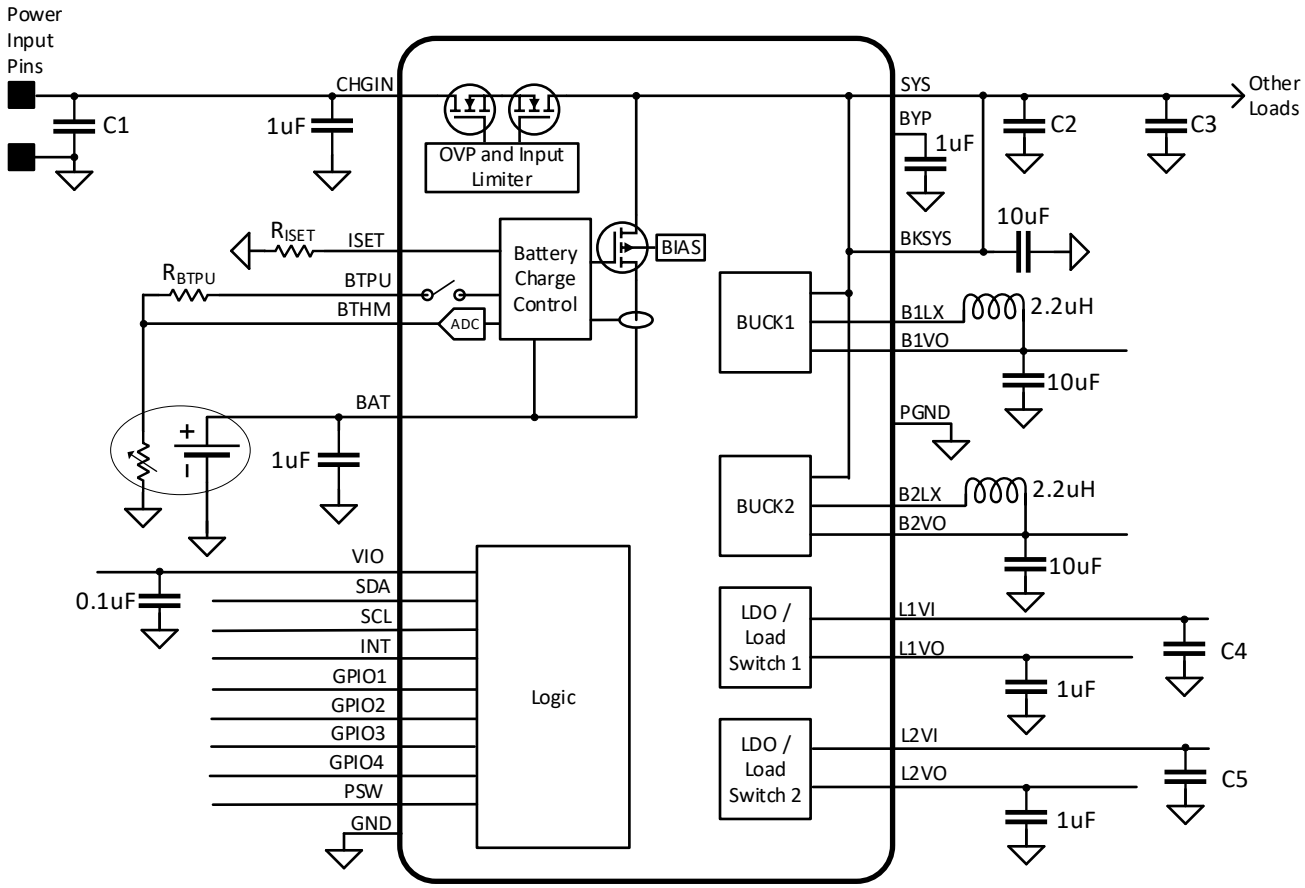
OTPInfo 0x2E

Bit	7	6	5	4	3	2	1	0
Name	OTPConfig							
Read/Write	RO							
Default	OTP							

Name	Bits	Description
OTPConfig	7:0	Unique code identifying the configuration settings in OTP

Application Information

OS100X is designed to require minimal external components but selection and placement of these passive components are important for proper operation.



Power Input

The power input source must include ESD protection which is provided by ceramic capacitor C1. If C1 is 0.1uF or larger, this pin will be protected against ESD up to IEC61000-4-2 15KV air gap and 8KV contact discharge provided there is a good PCB layout and GND connection. A total of 1uF effective bypass capacitance is required on the CHGIN input for stable operation of charger input but it may be split with the value of C1 as long as the capacitance close to CHGIN pin is at least 0.1uF

SYS Power Output

SYS power output must be bypassed with at least 10uF effective ceramic capacitance which may be split between C2 and C3. C2 must be at least 4.7uF effective and must have connections to SYS and GND with PCB traces as short as possible.

BKSYS Power Input

BKSYS power input must be bypassed with at least 10uF effective ceramic capacitance with PCB traces as short as possible between BKSYS and PGND.

ISET Resistor

A resistor (R1) is connected between ISET and GND top set the maximum charge current. The signal on ISET is susceptible to external interference and should be as short as possible and not routed near high energy switching nodes (example B1LX and B2LX)

BTPU pullup resistor

The battery pack temperature is measured by the resistor ratio between R2 and the thermistor inside the battery. OS100X has an extremely flexible design which will support any thermistor type. R2 should be chosen to maximize the voltage swing from the lowest expected temperature to the highest expected temperature to maximize the accuracy of JEITA thresholds and the 8bit ADC used to digitize the temperature value (if the battery thermistor is reused to measure system temperature). A good initial value to consider is the 25C resistance value of the thermistor.

VIO Bypass Capacitor

VIO is only used to power the I/O buffers and it requires a 0.1uF ceramic capacitor placed close to the VIO pin. Large currents may flow from VIO if large capacitive loads are placed on any of the GPIO output pins.

Buck Regulator Passive Components and Layout

Inductor selection for OS100X should be optimized for the application and a 2.2µH inductor is strongly recommended. For applications for which area is at premium, a 1µH inductor is acceptable, but will result in decreased efficiency.

In selecting the inductor, DC resistance (DCR), maximum current and saturation current should be considered. Lower DCR results in improved efficiency so for maximum efficiency, select an inductor with the lowest DCR for the allowed package size. A second factor to consider is magnetic loss whish is lower in inductors with larger physical size and higher saturation current rating. If possible, avoid ferrite inductors, as they usually exhibit poor AC characteristics.

The maximum current in the inductor is the sum of the maximum expected load current plus the peak value of the ripple current dependent on the operating condition.

Current ripple can be calculated as:

$$I_{ripple} = \frac{(V_i - V_o)}{L} T_{ON}$$

$$T_{ON} = \frac{V_o}{V_i} * 250ns * Adj$$

where V_o is the buck output voltage, V_i is the buck input voltage and Adj is the T_{ON} adjustment coefficient as programmed in Buck1/2ton registers.

The peak inductor operating current can thus be calculated as

$I_{Peak\_DCM} = I_{ripple} + I_{DC}$ for DCM

$$I_{Peak\_CCM} = \frac{I_{ripple}}{2} + I_{DC} \text{ for CCM}$$

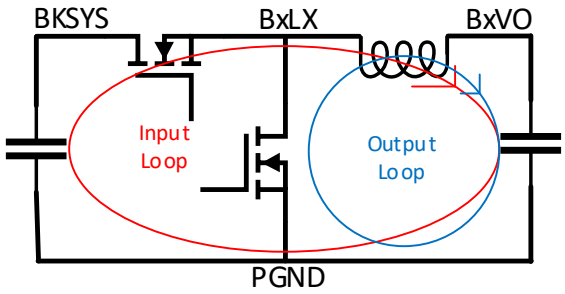
Where I_{DC} is the maximum expected load current for the application.

Recommended Buck Inductors

Optimization	Vendor	Part Number
Highest Efficiency	Murata	DFE201610E-2ER2M
Smallest Footprint	Murata	DFE18SBN2R2MEL

The output capacitor must be at least 10uF effective ceramic capacitance.

PCB layout is important to minimize radiated noise and maintain optimum performance. It is important to minimize the loop size for the input and output loops.



LDO regulator

The LDO and load switches require a minimum 1uF effective ceramic input capacitor but this may be shared with the power source feeding the input pins as long as the capacitor is within 1cm of the pin. The output must be bypassed with 1uF effective ceramic capacitance to GND with short PCB traces.

Ordering Information

Part Number

Part Number	Variant		Package Code
OS100X	“v”	-	WAA

Ordering Information

Part Number	Package	Packing Method	Minimum Order Quantity
OS100Xv-WAA	30WLCSP	Tape and Reel	5000

Variants OS1000

		Variant Value of register as defined by OTP configuration					
Register	**Name**	**A**	**B**	**C**	**D**	**E**	**F**
0x00	DeviceRev	0000 0XXX					
0x0A	ChargeCtrl1	1011 0011					
0x0B	ChargeCtrl2	X100 0001					
0x0C	ChargeCtrl3	0010 1001					
0x0D	ChargeCtrl4	0111 1111					
0x0E	ChargeCtrl5	XX10 1110					
0x0F	LDOCtrl	0100 1000					
0x10	LDO1Voltage	1100 0000					
0x11	LDO2Voltage	0000 0000					
0x12	Buck1Ctrl1	011X XXX0					
0x14	Buck1Ctrl3	1111 1111					
0x18	Buck2Ctrl1	011X XXX1					
0x1A	Buck2Ctrl3	1000 1010					
0x1E	IOCfg1	XX11 1111					
0x1F	IOCfg2	XX10 0100					
0x20	Config1	XX00 1110					
0x22	Config3	XXX0 1111					
0x23	Config4	XX00 1010					
0x24	Config5	XX00 0000					
0x25	JEITAConfig1	0010 0110					
0x26	JEITAConfig2	0011 0010					
0x27	JEITAConfig3	0110 1100					
0x28	JEITAConfig4	1001 0101					
0x29	JEITAConfig5	1110 1110					
0x2E	OTPInfo	0101 0101					
Power Up State*		Enabled					

“X” indicated a bit that is not set by OTP and may be different depending on OTP setting or device options

*Default state when battery with voltage greater than $V_{SYSUVLO}$ is attached

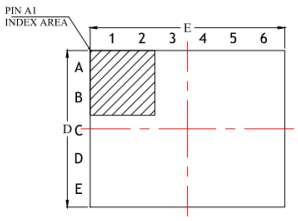
Variants OS1001

		Variant Value of register as defined by OTP configuration					
Register	**Name**	**A**	**B**	**C**	**D**	**E**	**F**
0x00	DeviceRev	1000 1XXX					
0x0A	ChargeCtrl1	0110 1110					
0x0B	ChargeCtrl2	X011 1101					
0x0C	ChargeCtrl3	0000 0000					
0x0D	ChargeCtrl4	0111 1111					
0x0E	ChargeCtrl5	XX10 1110					
0x0F	LDOCtrl	00XX 00XX					
0x10	LDO1Voltage	0000 0000					
0x11	LDO2Voltage	0000 0000					
0x12	Buck1Ctrl1	011X XXX1					
0x14	Buck1Ctrl3	1000 1111					
0x18	Buck2Ctrl1	011X XXX0					
0x1A	Buck2Ctrl3	1101 0100					
0x1E	IOCfg1	XX01 1000					
0x1F	IOCfg2	XX00 0000					
0x20	Config1	XX00 1111					
0x22	Config3	XXX1 0011					
0x23	Config4	XX00 0001					
0x24	Config5	XX00 0000					
0x25	JEITAConfig1	0011 1011					
0x26	JEITAConfig2	0101 0100					
0x27	JEITAConfig3	1001 1000					
0x28	JEITAConfig4	1011 1011					
0x29	JEITAConfig5	0000 0000					
0x2E	OTPInfo	0110 0110					
Power Up State*		Enabled					

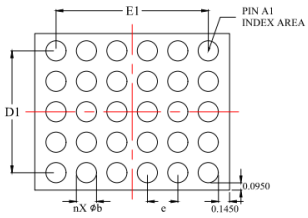
"X" indicated a bit that is not set by OTP and may be different depending on OTP setting or device options

* Default state when battery with voltage greater than $V_{SYSUVLO}$ is attached

Package Drawing



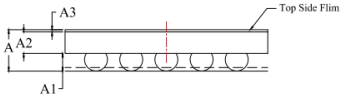
TOP VIEW



BOTTOM VIEW

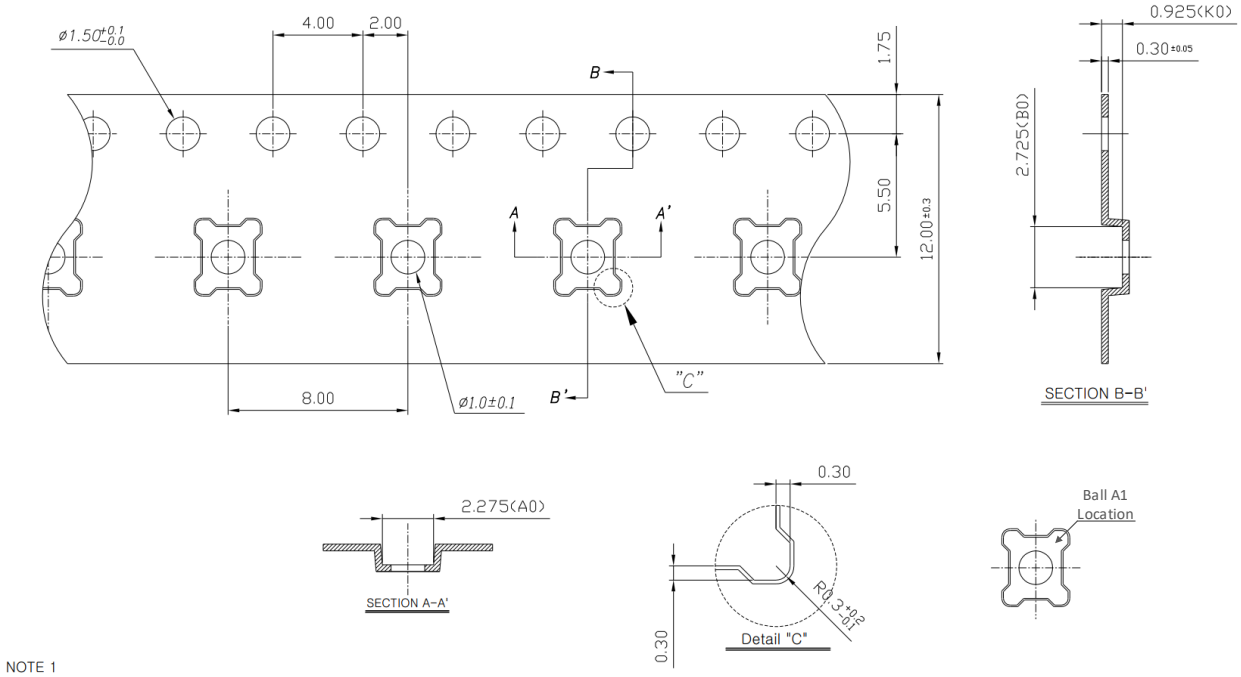
SYMBOL	DIMENSIONS		
	MIN	NOM	MAX
A	0.587	0.625	0.663
A1	0.180	0.200	0.220
A2	0.385	0.400	0.415
A3	0.022	0.025	0.028
E	2.525	2.555	2.585
D	2.025	2.055	2.085
E1	2.00 BSC		
D1	1.60 BSC		
e	0.40 BSC		
b	0.238	0.265	0.292
n	30		

All dimensions are in mm.



SIDE VIEW

Tape and Reel Details



NOTE 1

1. Material : Conductive Polystyrene
2. Camber not exceed 1mm in 250mm
3. A0 and B0 measured on a plane 0.3mm above the bottom of the pocket.
4. K0 measured from a plane on the carrier.
5. Pocket relative to sprocket hole measured as true position of pocket.
6. 10 sprocket hole pitch cumulative ±0.2
7. Pocket center and pocket hole center must be same position. (Tolerance : ±0.3mm)
8. Surface Resistability : 10E4 ~ 10E10 ohm/sq

Revision History

Rev1.4

- Corrected typos in text
- Removed unneeded ECTable entries
- Added variant A for OS1001
- Changed buck peak output current to Overload Current

Rev1.5

- Updated die size to 2.5x2.0mm
- Updated TOC for load regulation @ 1.2V to include load and high voltage ranges

Rev1.6

- Updated CHGINSt and CHGINOVPSt bit descriptions to reference values from Table 1
- Added note to CHGINSt register – interrupt only generated for 1 to 0 transition.
- Added Default State when battery attached to OTP option table
- Updated Figure 30 to show startup with button hold
- Figure 30 Exit Shelf Mode due to PSWb
- Added condition for Direct Mode that VCHGIN must be greater than VBAT
- Changed ESD rating from 2kV to 1.5kV HBM
- Added IEC61000 ESD ratings to CHGIN

RevA – Mass Production release

- Renamed CHGIN Direct Mode to Direct Mode
- Fixed text formatting in Direct Mode section
- Updated sequence needed to enter Direct Mode
- ECTable updates
    - CHGIN Direct Mode current
    - CHGIN to SYS resistance
    - LDO Iq and leakage IN to OUT